K22 – Operating Systems: Design Principles and Internals

Fall 2025 @dit

Vaggelis Atlidakis

Lecture 17

References: Similar OS courses @Columbia, @Stanford, @UC San Diego, @Brown, @di (previous years); and textbooks: Operating Systems: Three Easy Pieces, Operating Systems: Principles and Practice, Operating System Concepts, Linux Kernel Development, Understanding the Linux Kernel

TOP 20 RESEARCH UNIVERSITIES IN EASTERN EUROPE BY CITATION RANK (OUT OF 796)[1]

DATA SOURCES: **GOOGLE SCHOLAR** AND **WEBOMETRICS RANKING**,[2] JAN. 2025

CITATION RANK		HIGHER EDUCATION INSTITUTION (HEI)	COUNTRY	CITATIONS
EASTERN EUROPE (796 HEIs)	WORLD (6,191 HEIs)			
1	85	National and Kapodistrian University of Athens / Εθνικό και Καποδιστριακό Πανεπιστήμιο Αθηνών	Greece	4,864,139
2	264	Aristotle University of Thessaloniki / Αριστοτέλειο Πανεπιστήμιο Θεσσαλονίκης	Greece	2,182,896
3	388	University of Tartu / Tartu Ülikool	Estonia	1,498,293
4	395	University of Patras / Πανεπιστήμιο Πατρών	Greece	1,476,112
5	425	National Technical University of Athens / Εθνικό Μετσόβιο Πολυτεχνείο	Greece	1,346,248
6	436	University of Crete / Πανεπιστήμιο Κρήτης	Greece	1,308,661
7	451	Hacettepe University / Hacettepe Üniversitesi	Turkey	1,248,796
8	456	National Research University Higher School of Economics / Национальный исследовательский университет Высшая школа экономики	Russia	< 1,240,618
9	483	Eötvös Loránd University Budapest / Eötvös Loránd Tudományegyetem ELTE	Hungary	1,148,651
10	484	University of Ljubljana / Univerza v Ljubljani	Slovenia	1,147,135
11	487	University of Thessaly / Πανεπιστήμιο Θεσσαλίας	Greece	1,134,957
12	501	Charles University in Prague / Univerzita Karlova v Praze UK	Czechia	1,089,590
13	513	University of Ioannina / Πανεπιστήμιο Ιωαννίνων	Greece	1,054,433

Overview

- We'll start from hardware and follow a question-oriented approach
  - ~~Intro [Q: What is an OS?]~~
  - ~~Events [Q: When does the OS run?]~~
  - ~~Runtime [Q: How does a program look like in memory?]~~
  - ~~Processes [Q: What is a process?]~~
  - ~~IPC [Q: How do processes communicate?]~~
  - ~~Threads [Q: What is a thread?]~~
  - ~~Synchronization [Q: What goes wrong w/o synchronization?]~~
  - ~~Time Management [Q: What is scheduling?]~~
  - **Memory Management [Q: What is virtual memory?]**
  - Files [Q: What is a file descriptor?]
  - Storage Management [Q: How do we allocate disk space to files?]

* Basic (H/W & S/W)
* Abstractions
* Primitives
* **Mechanisms**

Overview

- **Memory management**
  - **Q1**: What is virtual memory?
  - **Q2**: Why is virtual memory necessary?
  - **Q3**: How is virtual memory implemented?

  ...

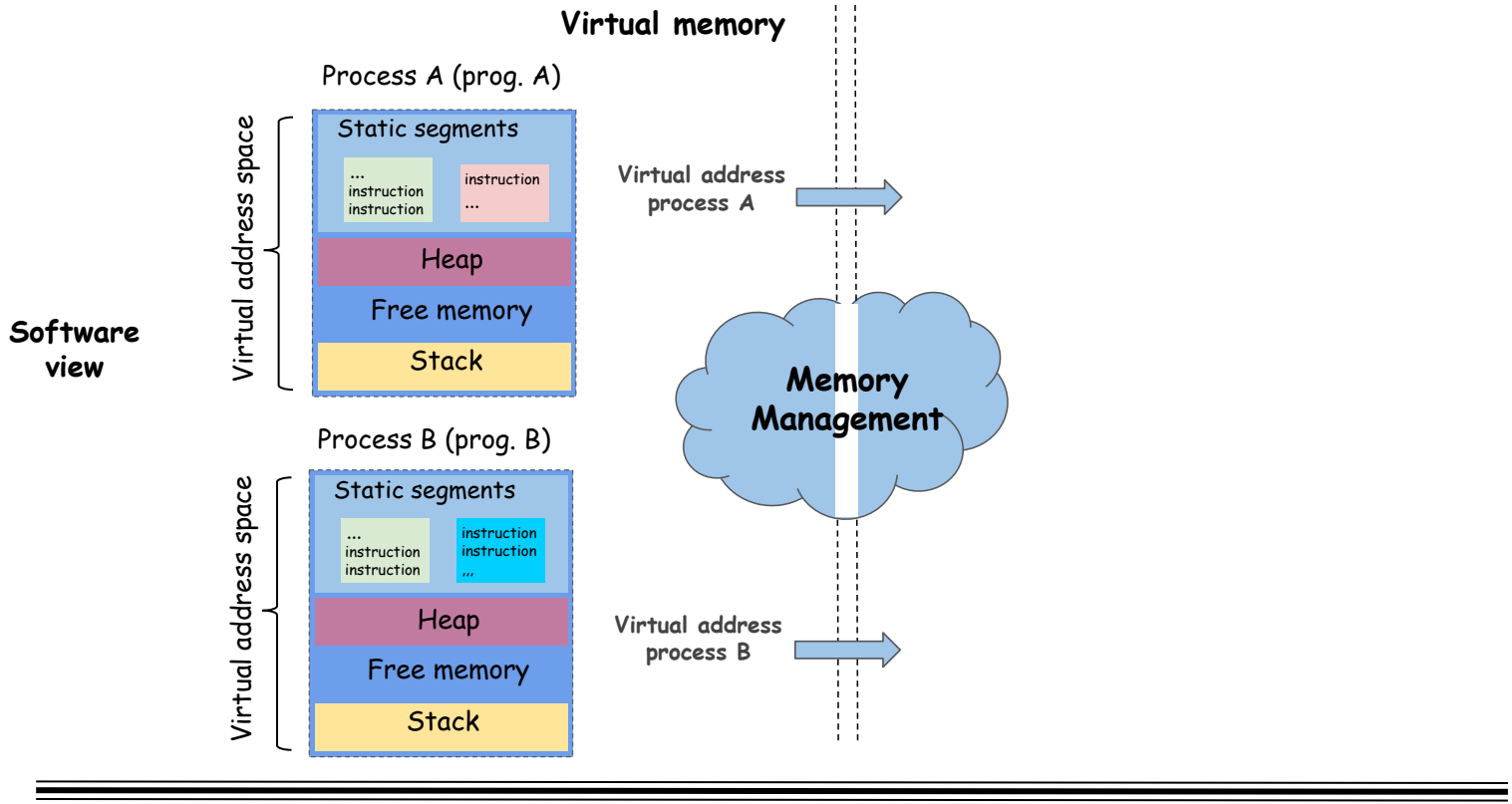
What is virtual memory?

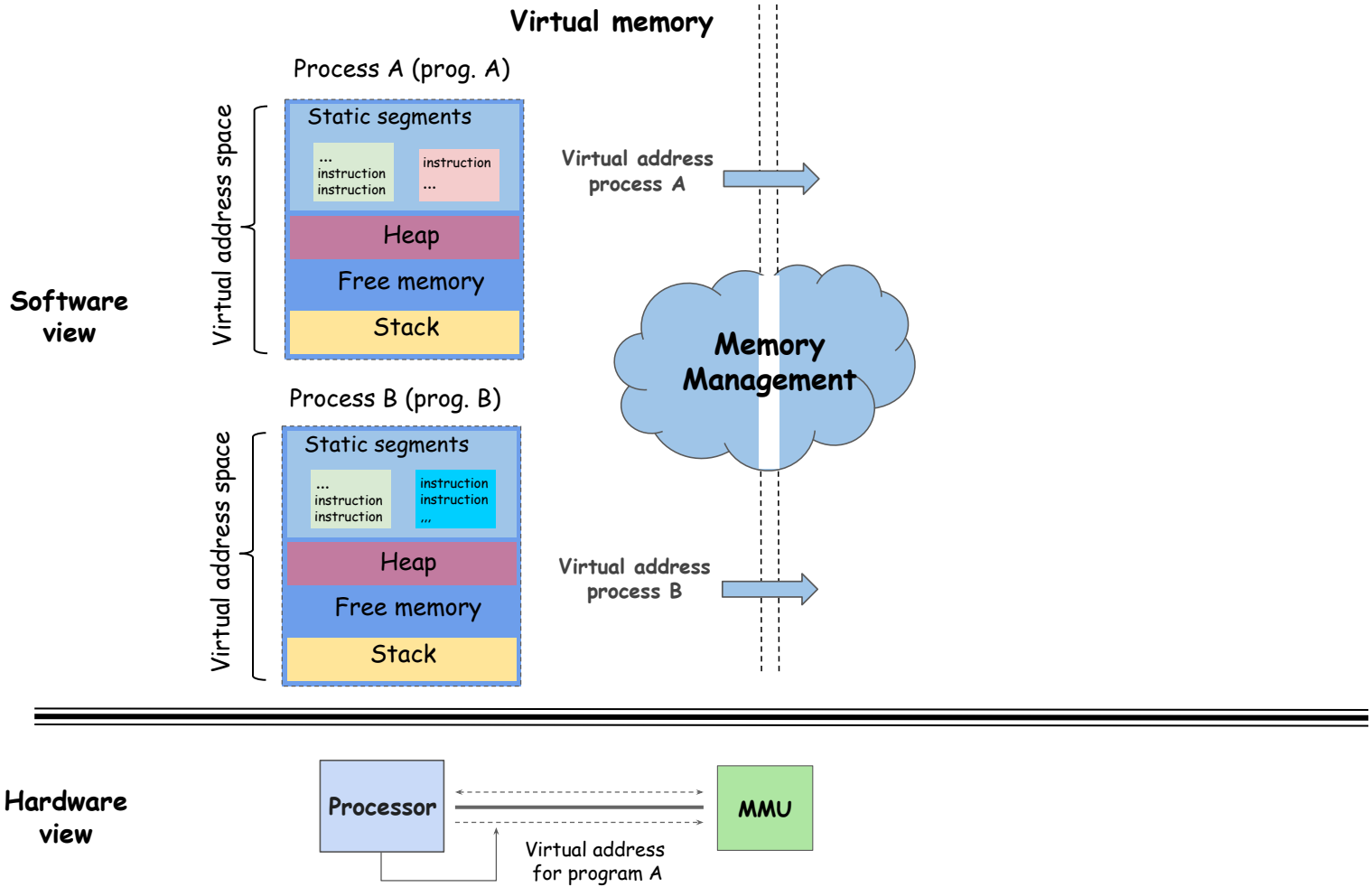
>> A layer of abstraction

- Translates virtual addresses into physical addresses

  - **Virtual addr.**: the language processes talk to the processor about memory
  - **Physical addr.**: the language actual contents of memory are accessed

- The way programmers imagine programs interact with memory is an illusion on top of the virtual memory abstraction layer


Virtual memory
Process A (prog. A)
Virtual address space
Static segments
... instruction instruction
instruction ...
Heap
Free memory
Stack
Virtual address process A
Memory Management
Process B (prog. B)
Virtual address space
Static segments
... instruction instruction
instruction instruction ,,,
Heap
Free memory
Stack
Virtual address process B
Software view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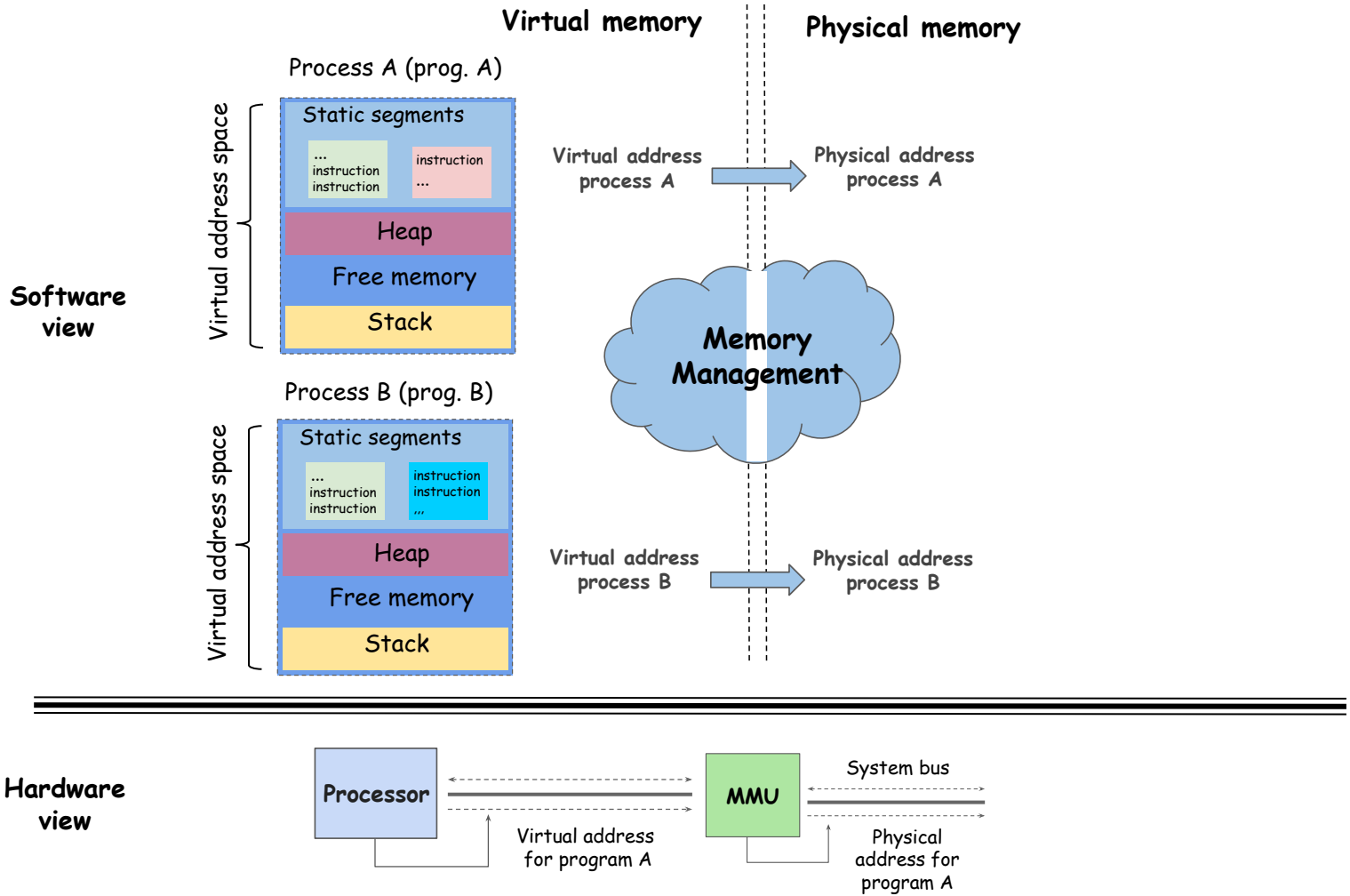
Virtual address process B
Software view
Hardware view
Processor
MMU
Virtual address for program A


Virtual memory
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Physical address process A
Memory Management
Process B (prog. B)
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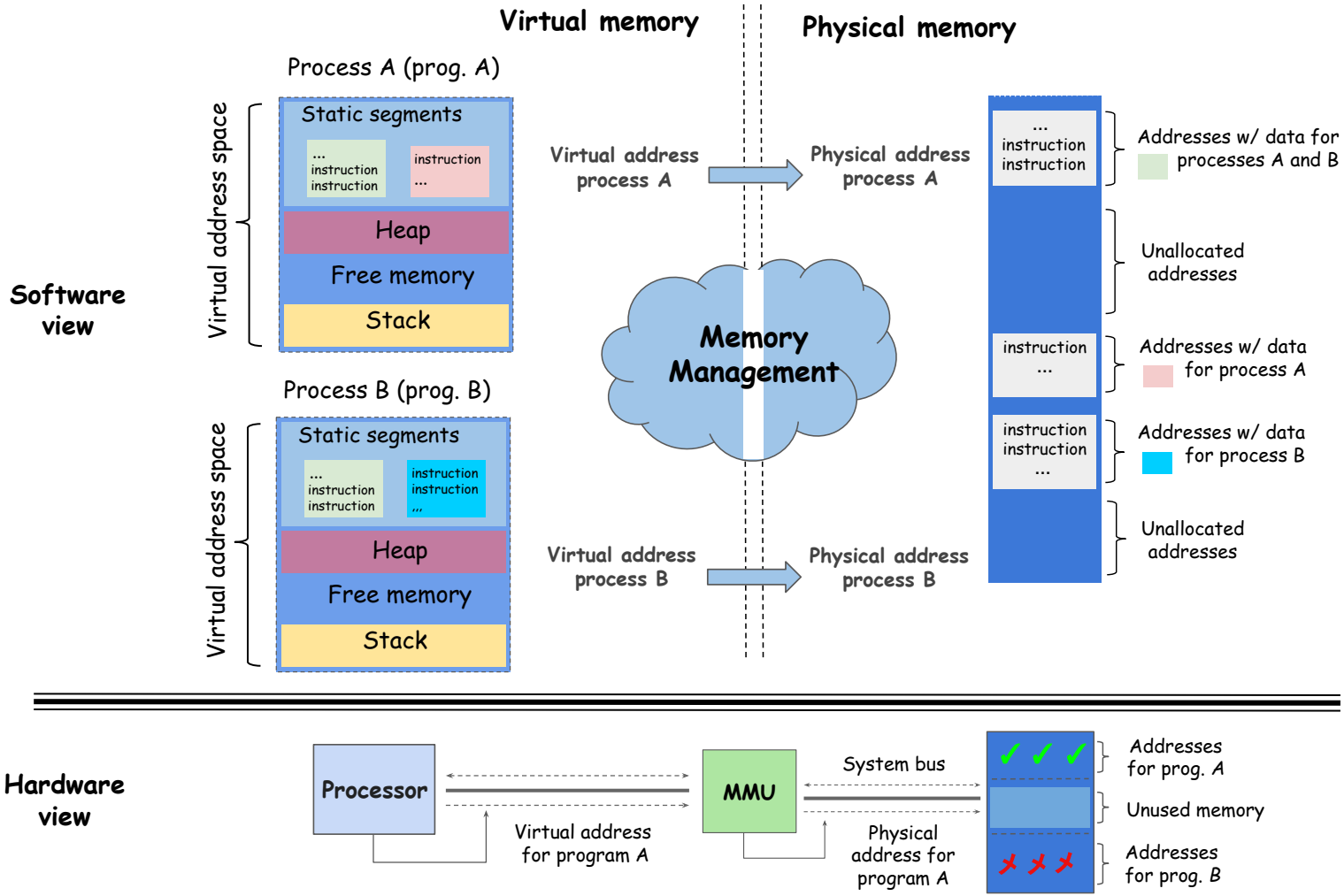
Stack
Virtual address process B
Physical address process B
Software view
Hardware view
Processor
Virtual address for program A
MMU
System bus
Physical address for program A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Virtual address space
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Free memory
Stack
Virtual address process A
Physical address process A
Virtual address process B
Physical address process B
Memory Management
... instruction instruction
Addresses w/ data for processes A and B
Unallocated addresses
instruction ...
Addresses w/ data for process A
instruction instruction ...
Addresses w/ data for process B
Unallocated addresses
Hardware view
Processor
Virtual address for program A
MMU
System bus
Physical address for program A
Addresses for prog. A
Unused memory
Addresses for prog. B

What is virtual memory? (demo)

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```c
#include <stdio.h>
#include <stdlib.h>
#include <time.h>
#include <unistd.h>

int main(int argc, char **argv) {
   int i;
   pid_t pid = getpid();

   i = atoi(argv[1]);

  printf("[PID: %d]; &i: %p; i: %d\n", pid, &i, i)
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```
➜ git:(master) ✗ echo 0 | sudo tee
/proc/sys/kernel/randomize_va_space
0

➜ vm git:(master) ✗ ./hello_vm 10 &
[1] 186394
[PID: 186394]; &i: 0xffffffff210; i: 10
[PID: 186394]: Seep for 10 sec

➜ vm git:(master) ✗ ./hello_vm 3 &
[2] 186432
[PID: 186432]; &i: 0xffffffff210; i: 3
[PID: 186432]: Sleep for 3 sec

➜ vm git:(master) ✗ [PID: 186432]; I am done now
[2] + 186432 done       ./hello_vm 3

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[1] + 186394 done       ./hello_vm 10
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[2] + 186432 done       ./hello_vm 3

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Same address different value, both programs running…

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- Performant use of resources
  - >> Programs have a memory footprint as much as the size of storage and run at speed close to the speed of CPU caches (how?...)
  - >> **CoW**: Laziness -> defering Vs. **Locality**: Proactivity -> prefetching

How is virtual memory implemented?

"We've rewritten the VM several times in the last ten years, and I expect it will be changed several more times in the next few years. Within five years, we'll almost certainly have to make the current three-level page tables be four levels, etc."

—Linus Torvald, 2001.

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Q1: What are the entries of the index?

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Q3: How are the entries of the index allocated?

Q4: How are the entries of the index replaced?

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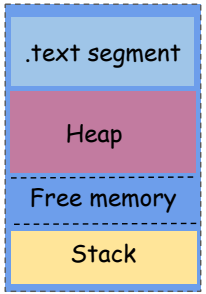
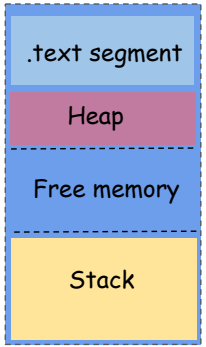
Mechanism: Segmentation

Virtual memory

Process A

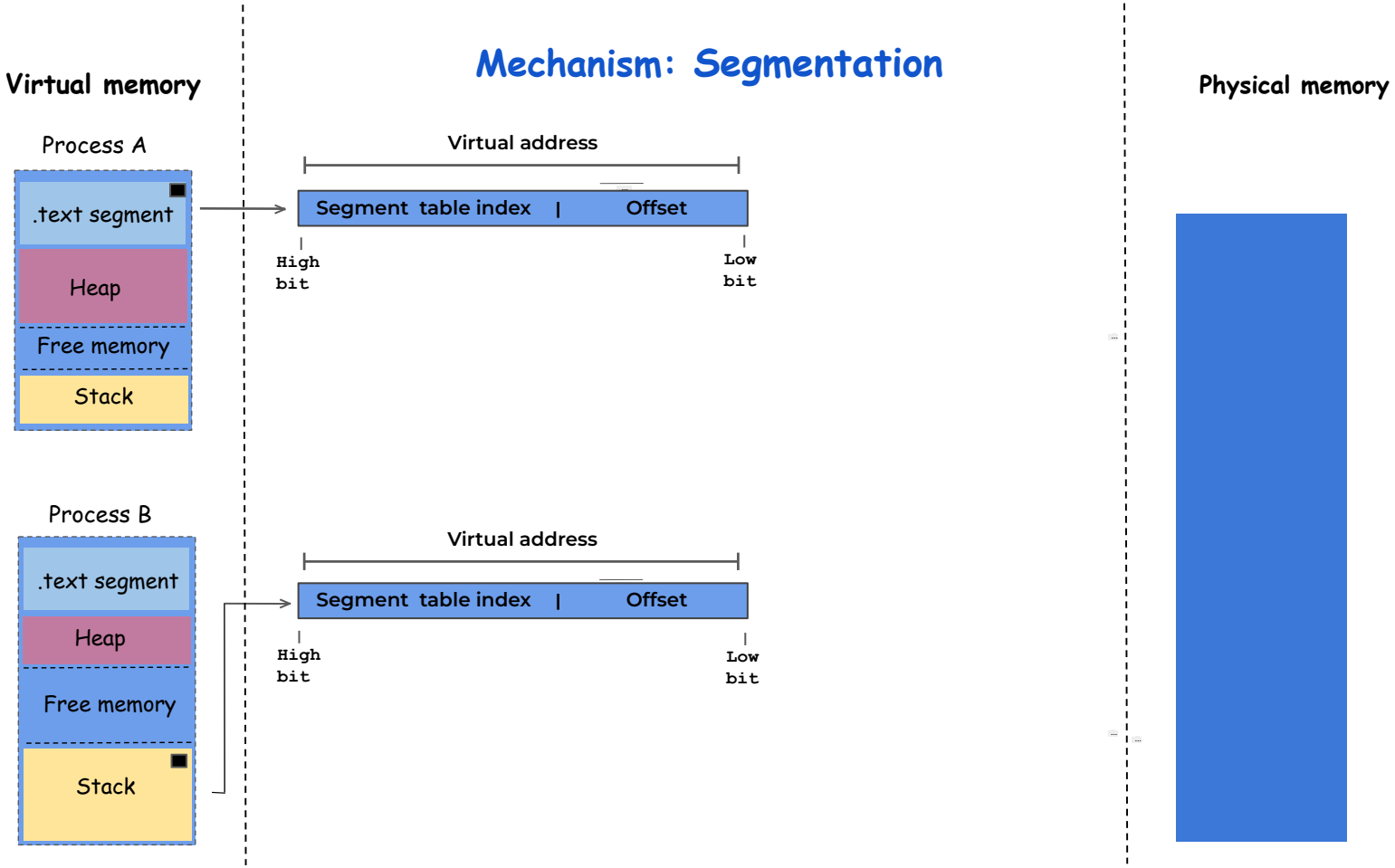


Process B



Physical memory

Mechanism: Segmentation



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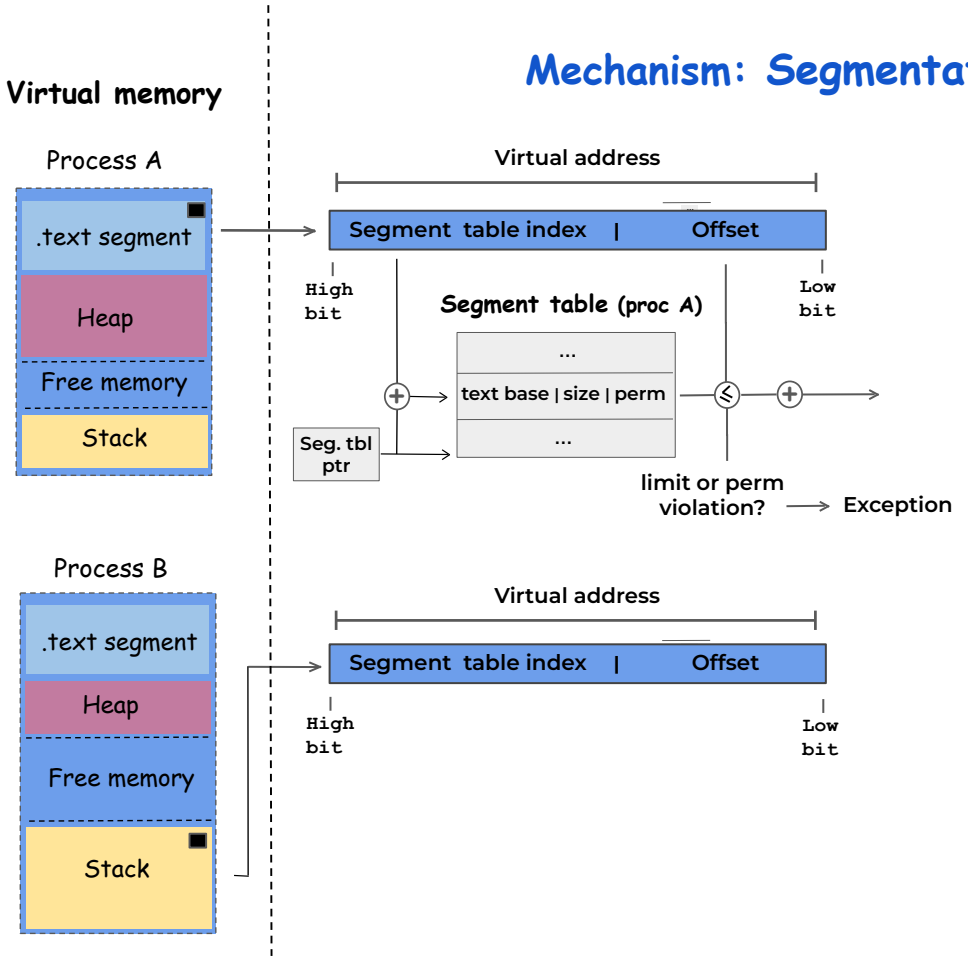

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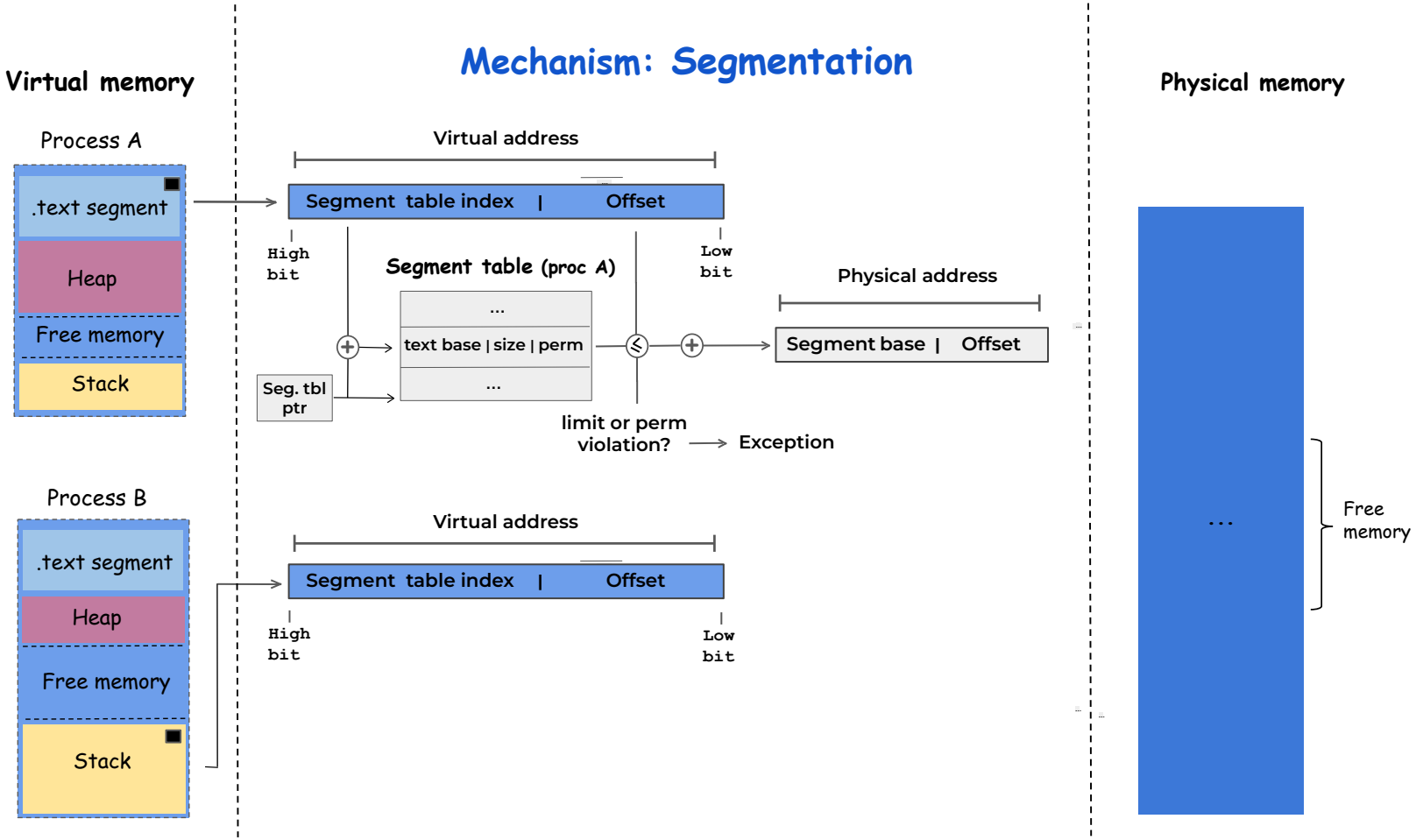

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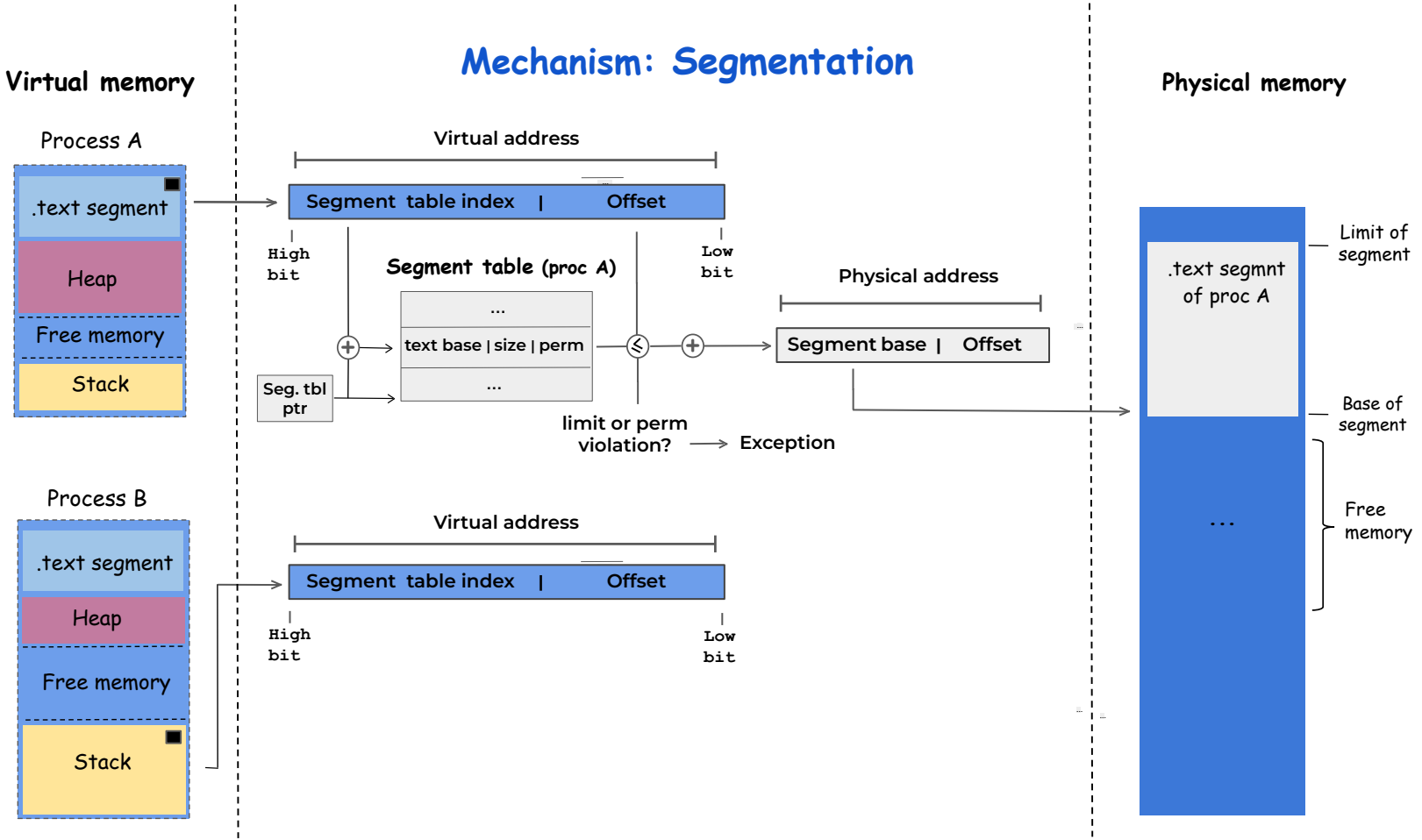

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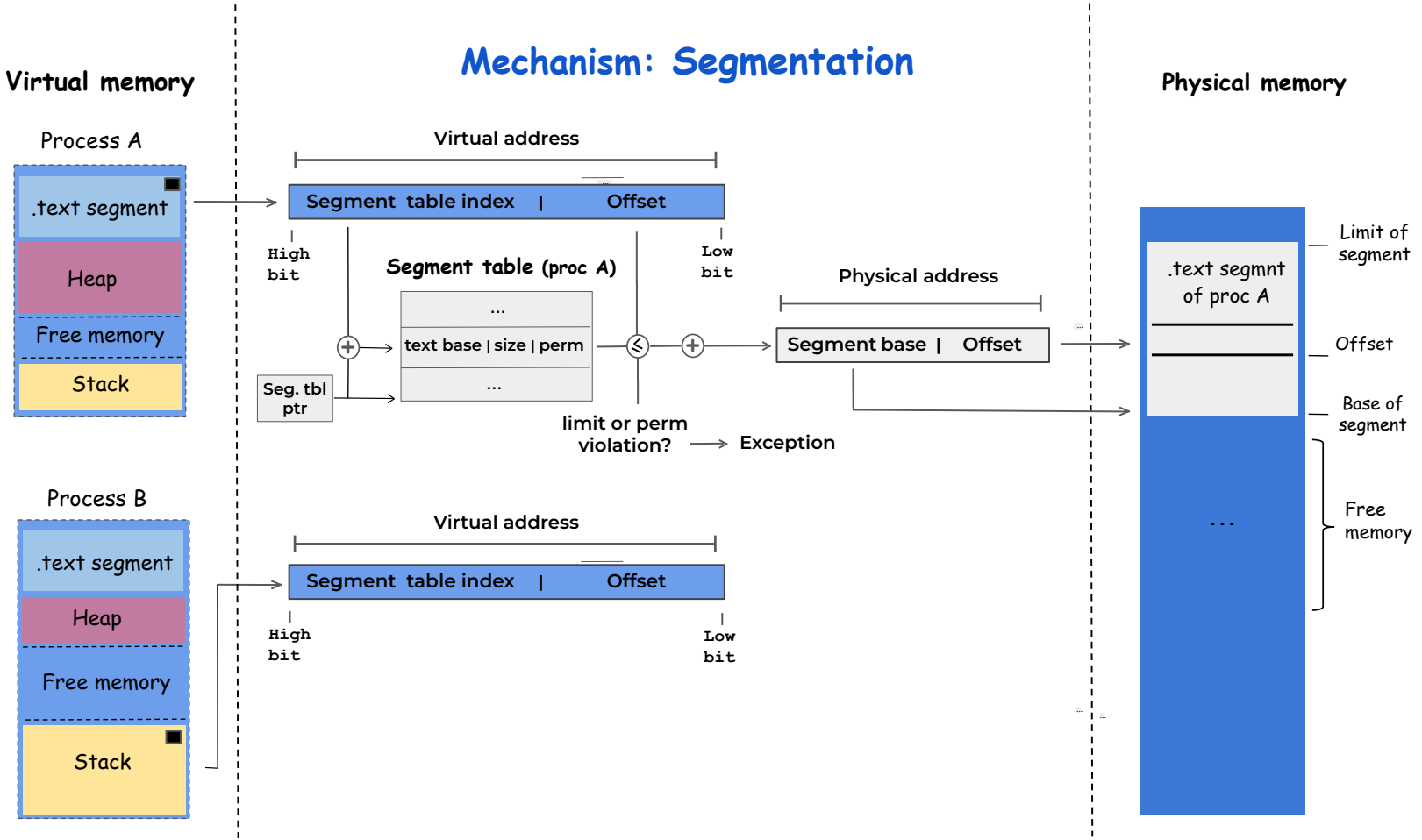

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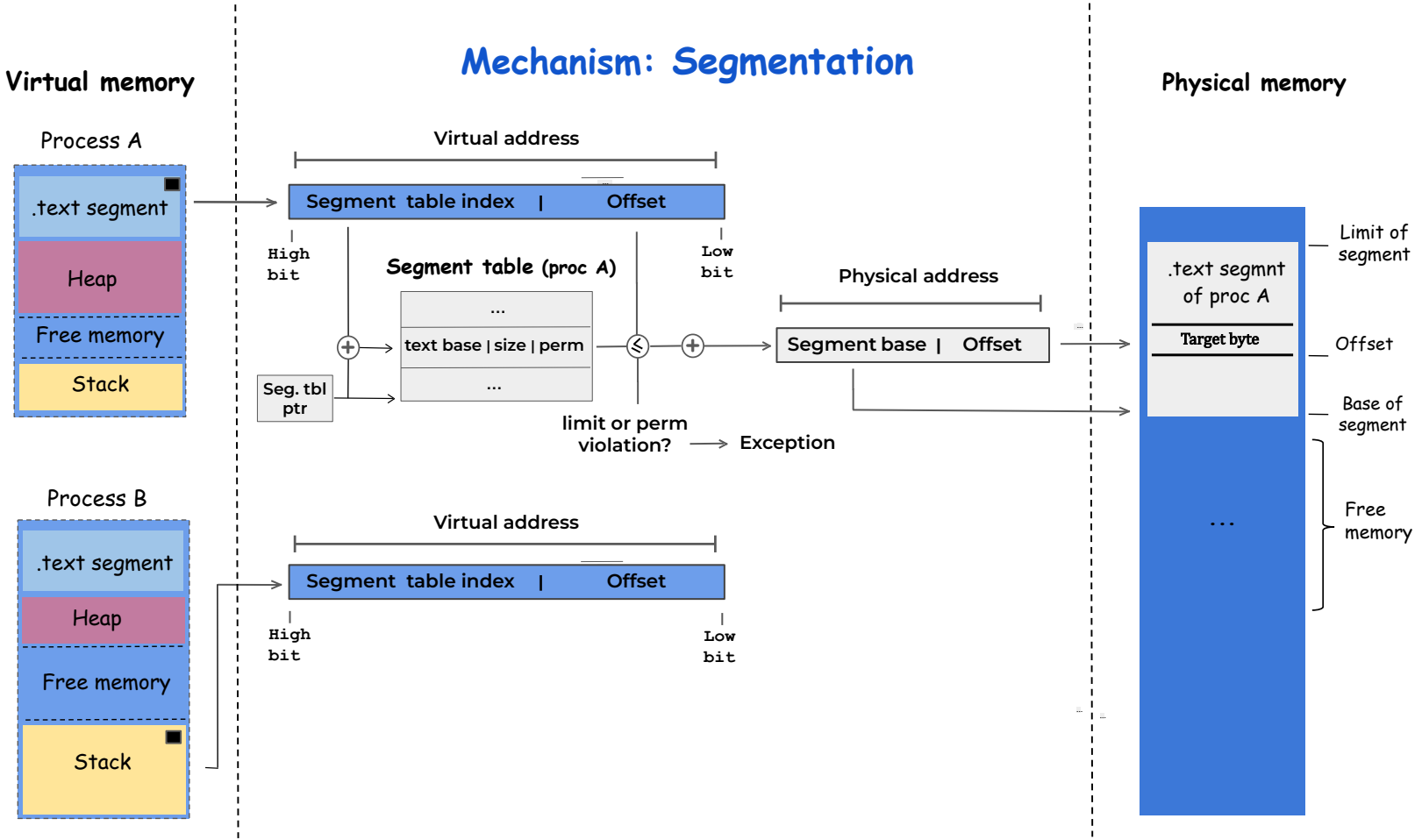

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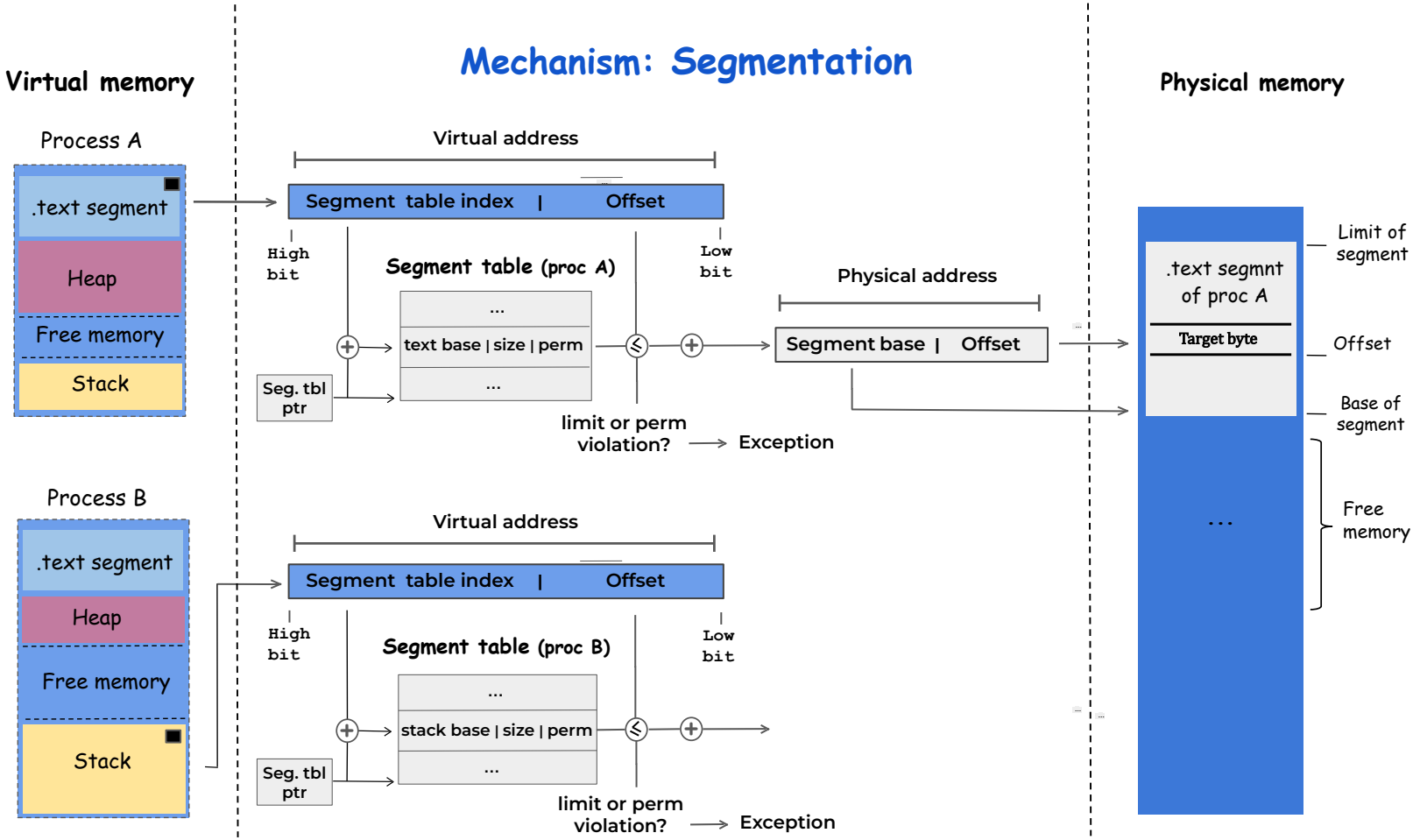

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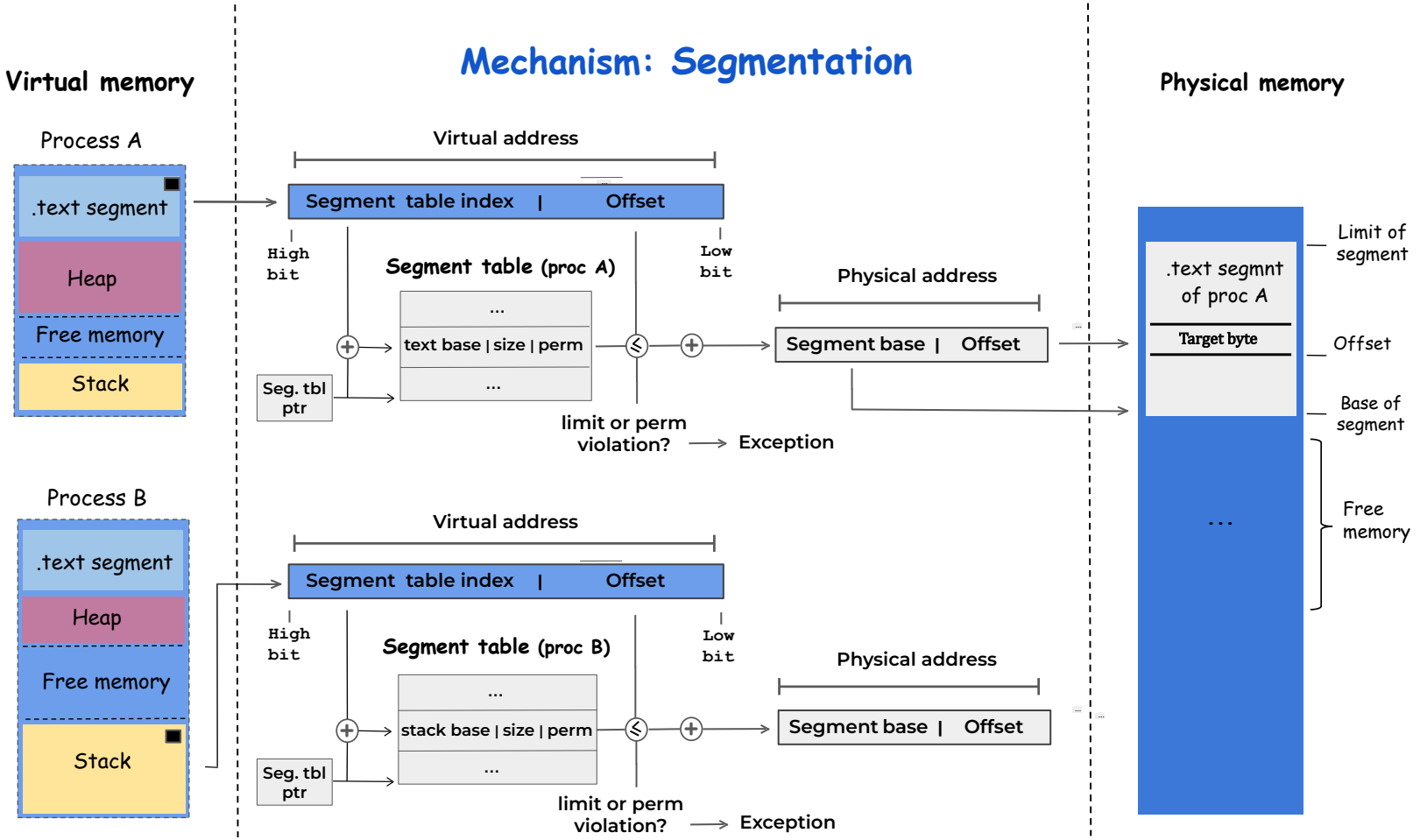

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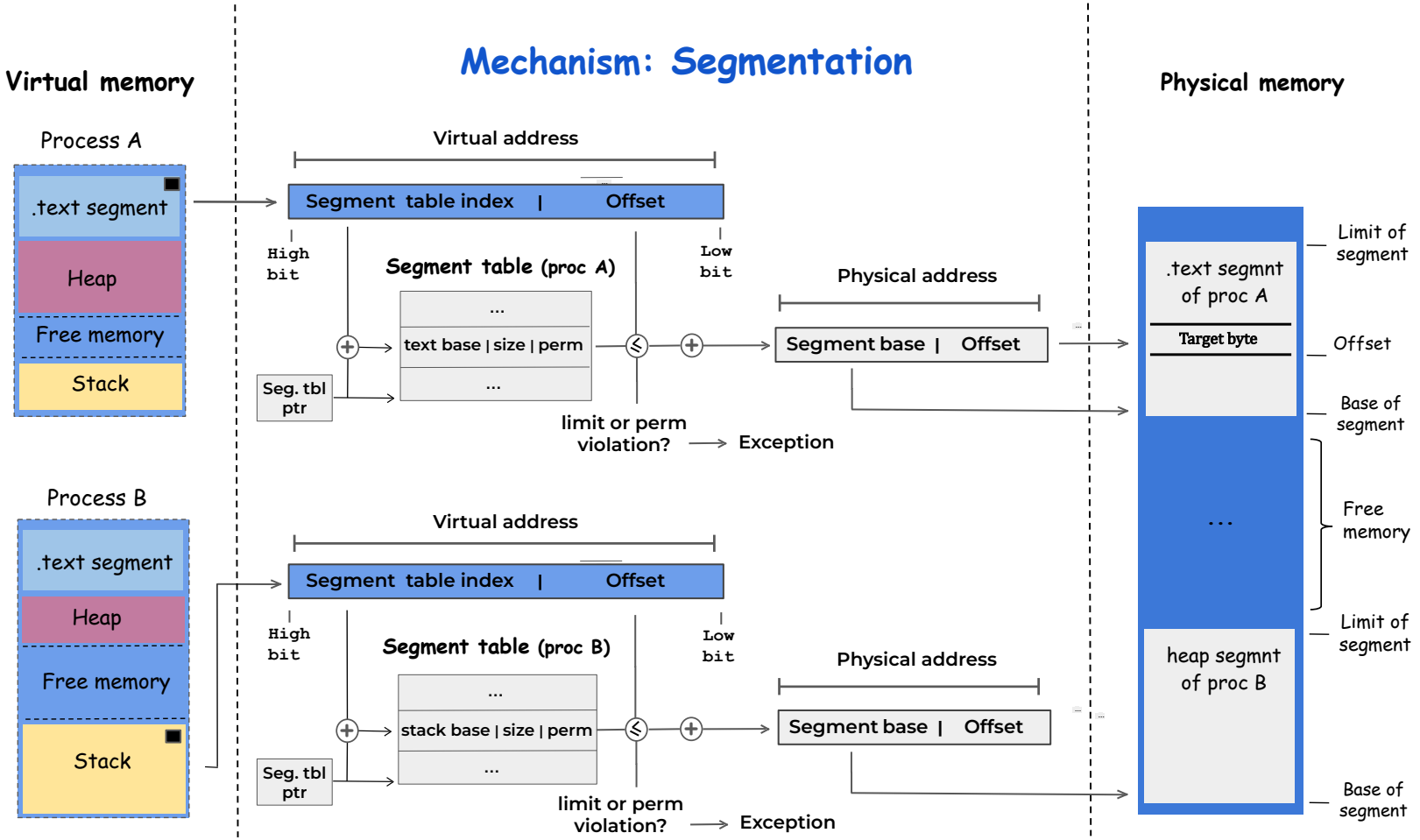

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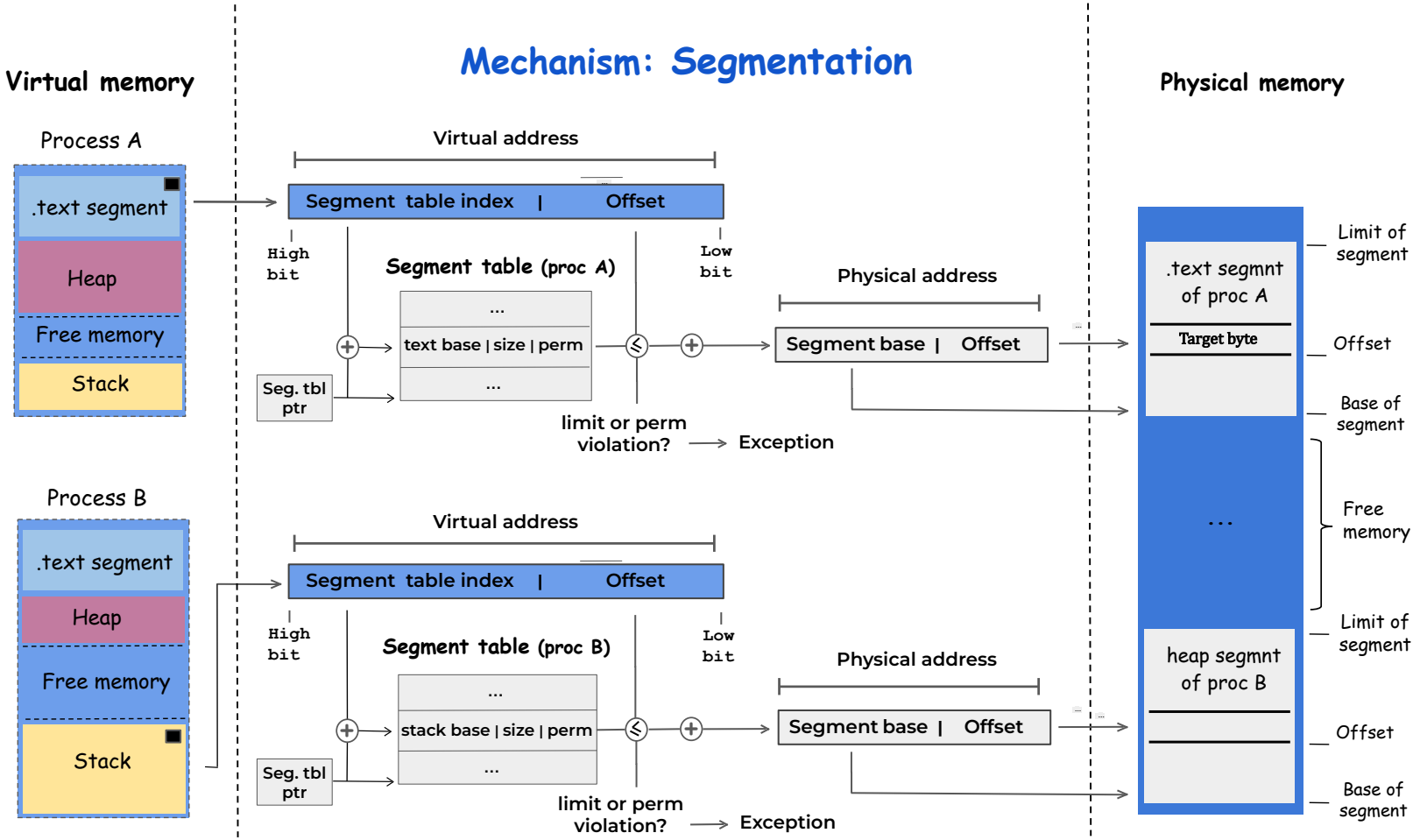

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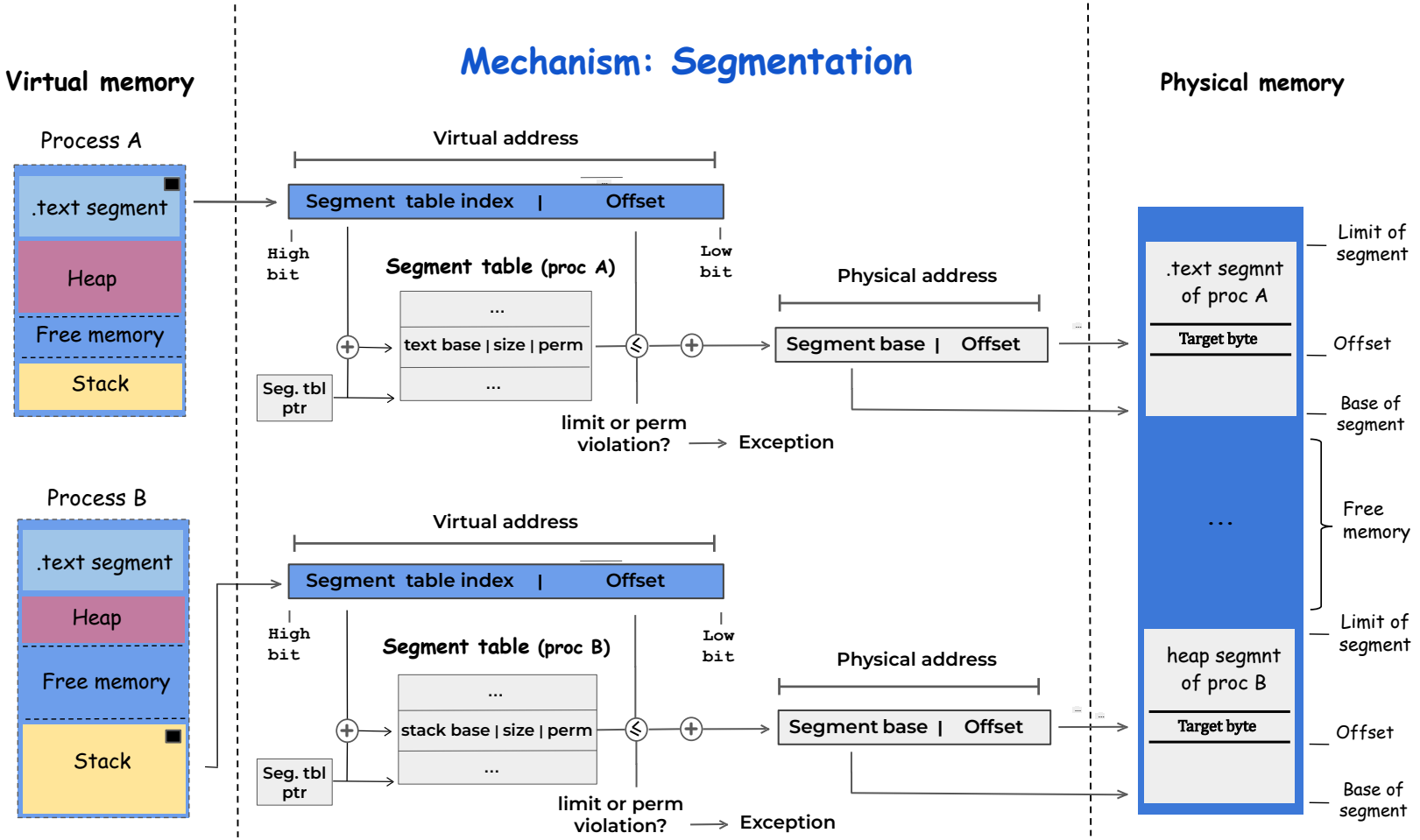

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› Assume 32-bit virtual and physical address space
w/ 8-bits for the segment table index (segment selector) and 24-bits for offset

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Segment table (process A)

Seg No	Base	Size	Perm
0	0x4f00000	0xffffff	rw-
1	0x0100000	0x1fffff	r-x
2	0x3000000	0x9fffff	r--

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Q3: What's the physical address for virtual address?

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  = [0100 11111] [0000 0000] [0001 0000] [0011 0000]
  = 0x4f 00 10 30 => 00 10 30 < 9f ff ff ? OK
  = 0x4f001030

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= [0011 0000] [1010 0010] [0000 0011] [0101 1111]
= 0x30 a2 03 5f => a2 03 5f < 9f ff ff ? NOT_OK

Mechanism: Segmentation

Limitations of Segmentation

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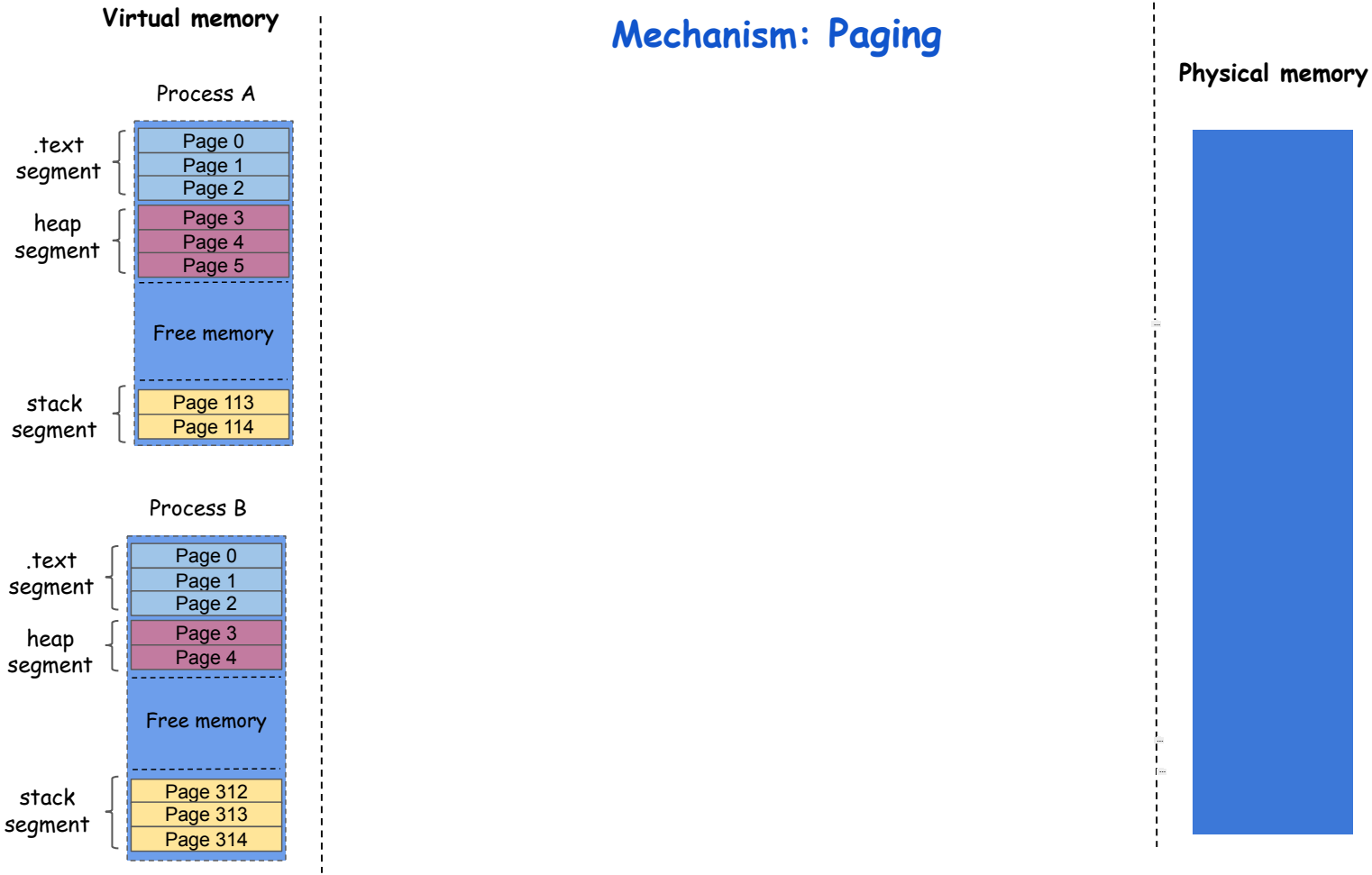
Mechanism: Segmentation

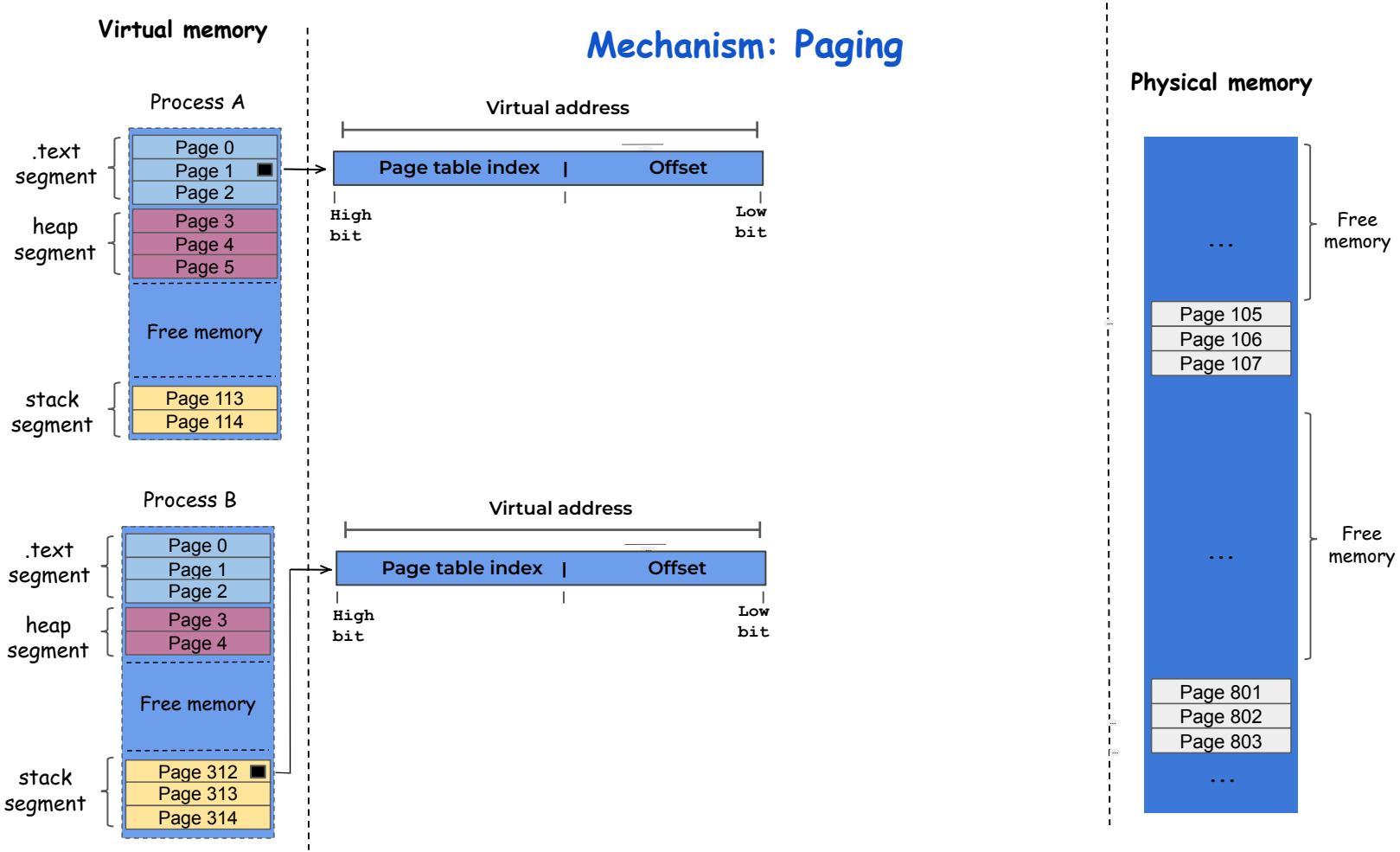
Limitations of Segmentation

- Fragmentation: Inability to use available memory
  - Internal fragmentation: Unused portions internally on each segment
  - External fragmentation: Free segments not usable due to unfit sizes

Mechanism: Paging



Mechanism: Paging



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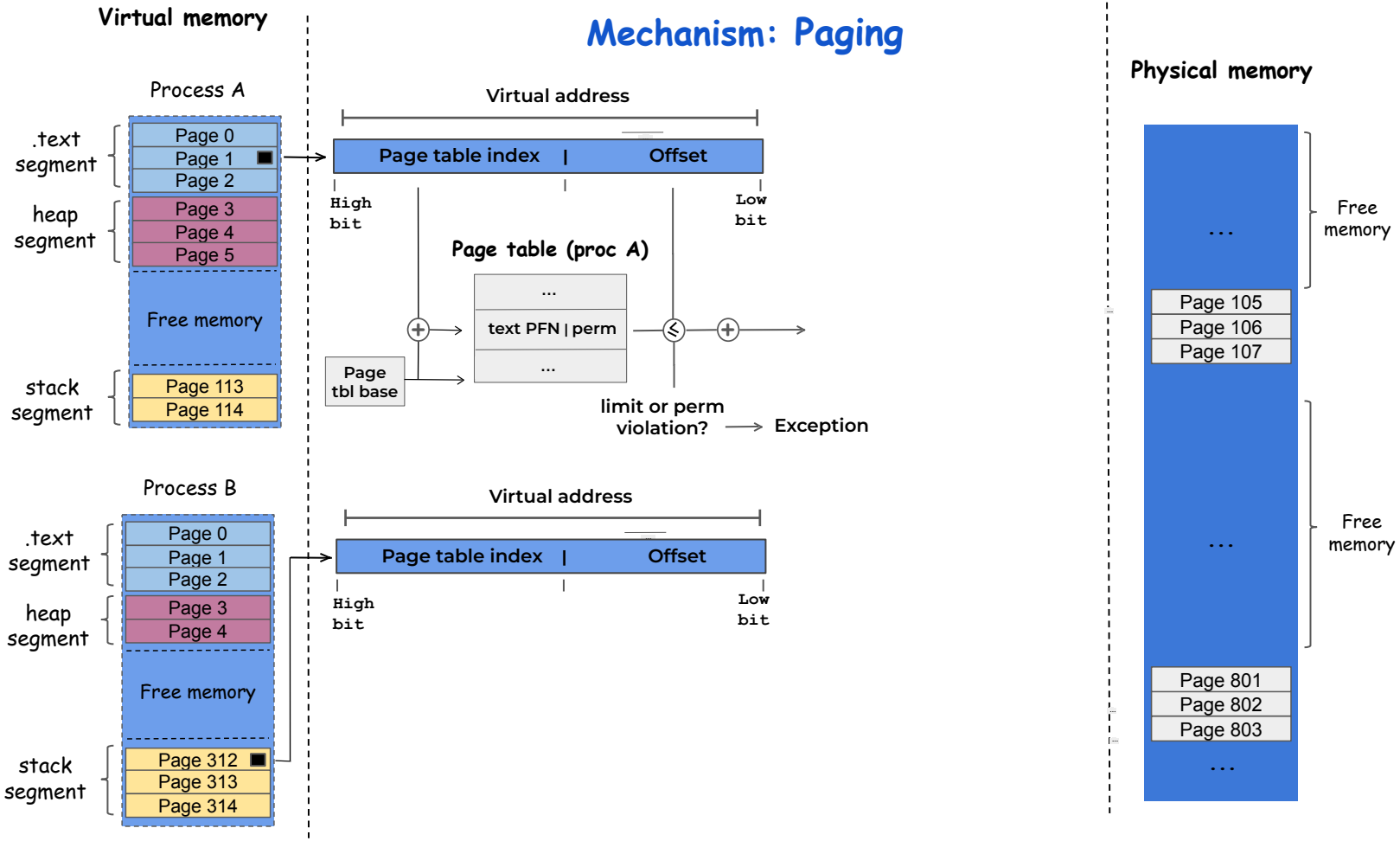

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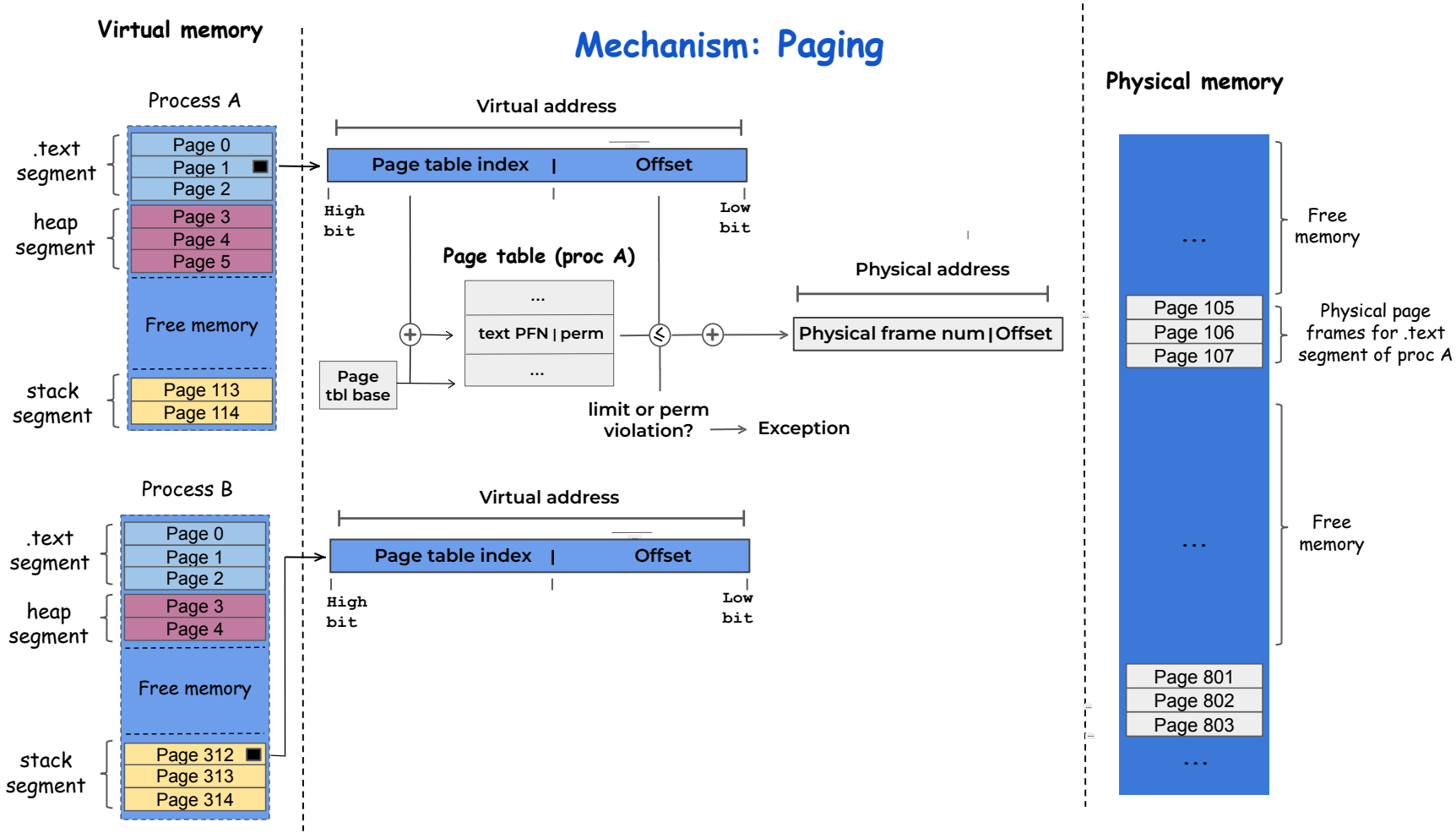

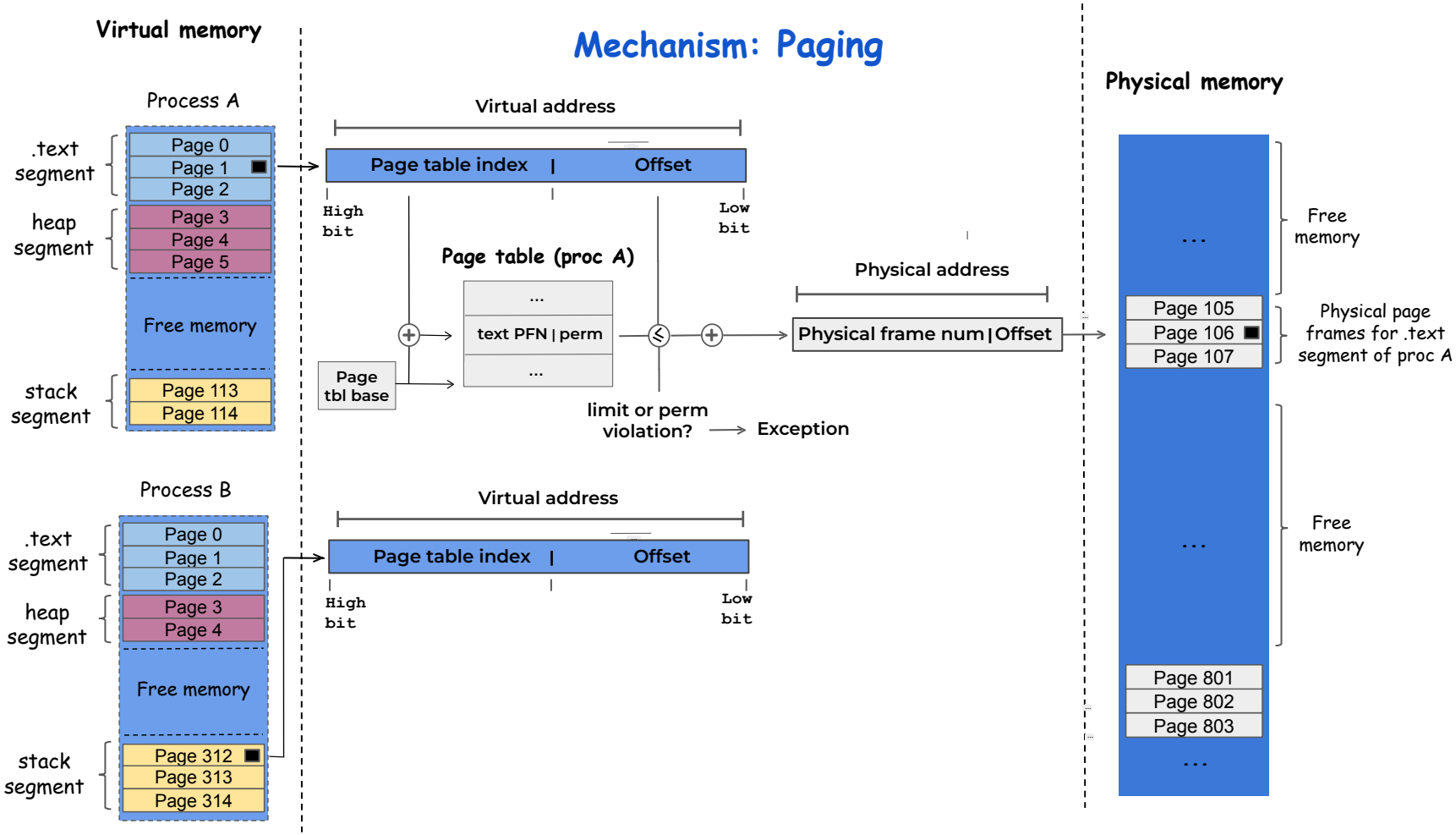
Mechanism: Paging
Virtual memory
Process A
.text segment
heap segment
stack segment
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Free memory
Page 113
Page 114
Virtual address
Page table index | Offset
High bit
Low bit
Page table (proc A)
...
text PFN | perm
...
Page tbl base
Physical address
Physical frame num | Offset
limit or perm violation?
Exception
Physical memory
...
Free memory
Page 105
Page 106
Page 107
Physical page frames for .text segment of proc A
...
Free memory
Page 801
Page 802
Page 803
...
Process B
.text segment
heap segment
stack segment
Page 0
Page 1
Page 2
Page 3
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Free memory
Page 312
Page 313
Page 314
Virtual address
Page table index | Offset
High bit
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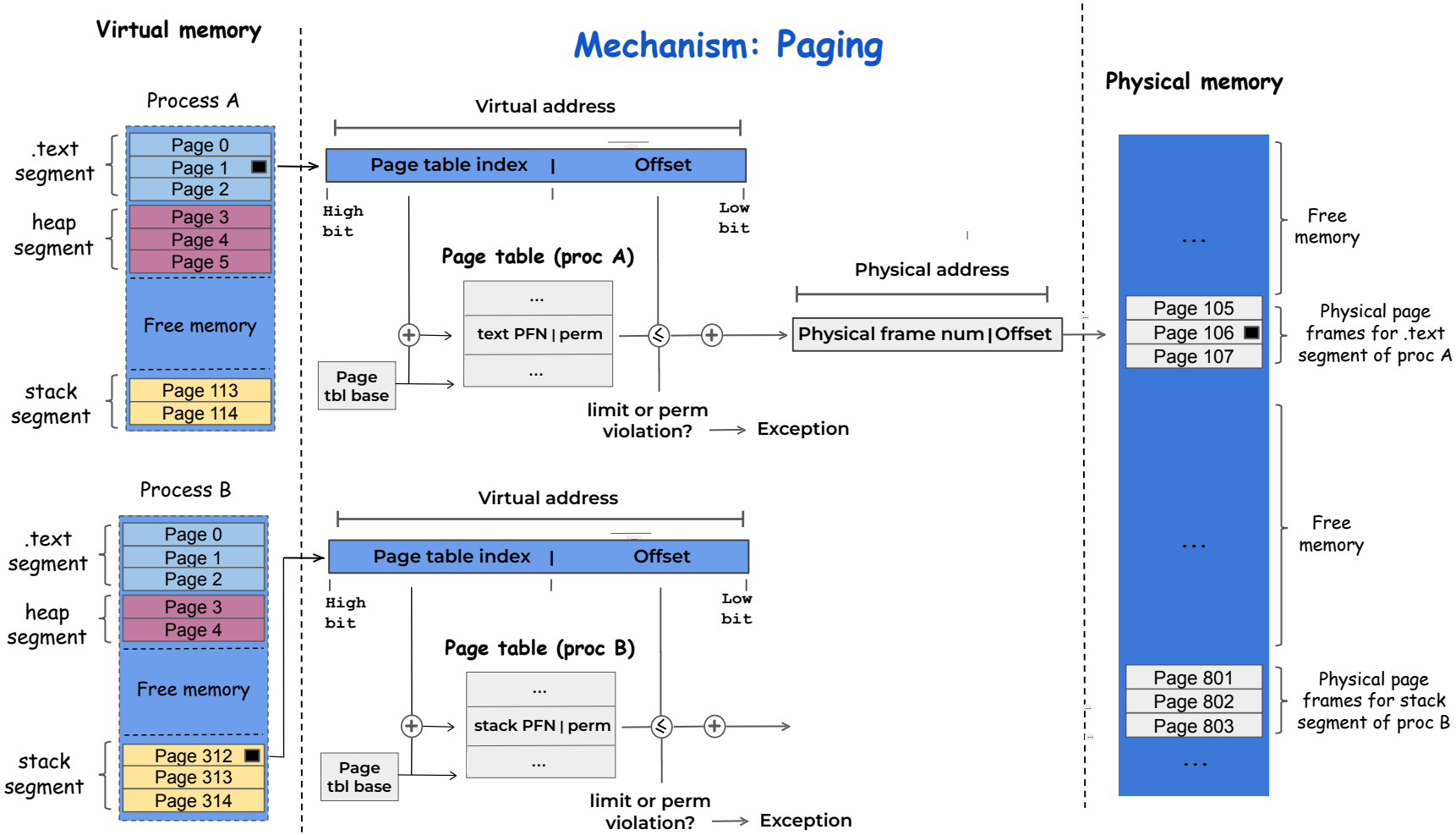
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...
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stack segment
Page 0
Page 1
Page 2
Page 3
Page 4
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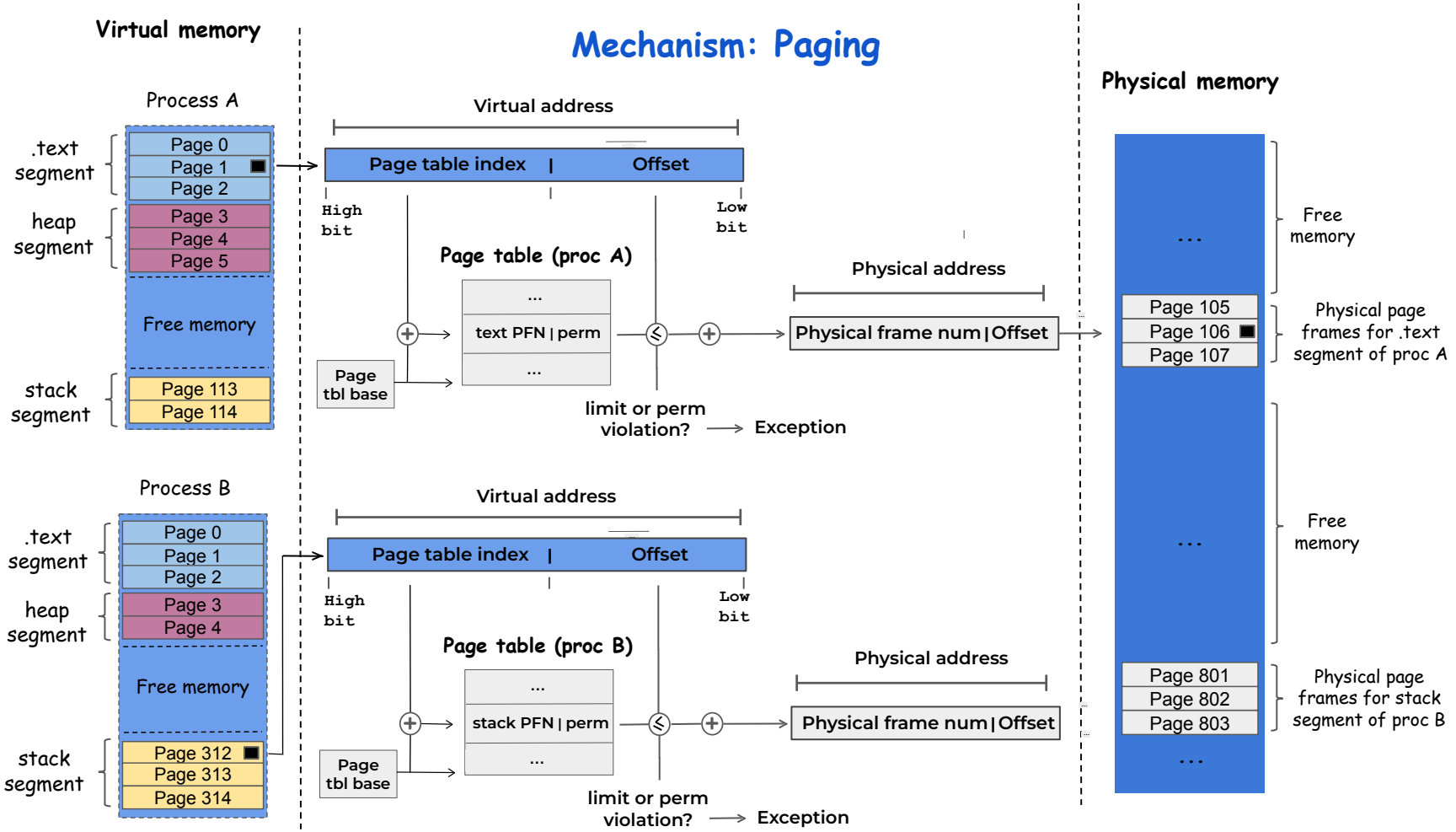
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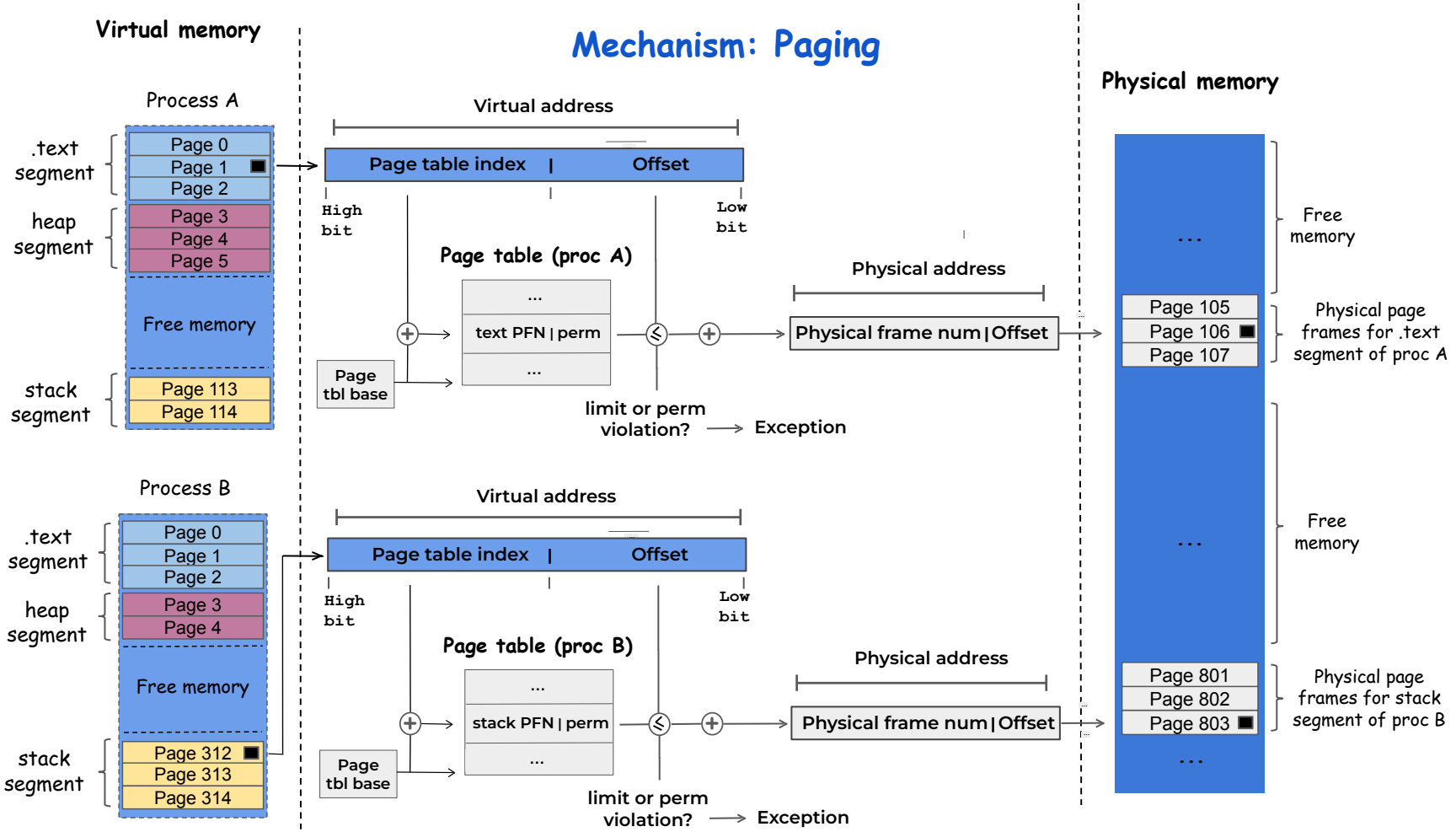
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Mechanism: Paging

› Assume 32-bit virtual and physical address space, 20-bits for page table index and 4KB pages (i.e., 12 bits for offset)

Q: What's the physical address for virtual address?

Page table (process A)

Index	PFN	Perm
0	302	rw-
1	106	r-x
2	19	r--

Mechanism: Paging

› Assume 32-bit virtual and physical address space, 20-bits for page table index and 4KB pages (i.e., 12 bits for offset)

Q: What's the physical address for virtual address?

- 0x00000400 =

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  = [0000 0000] [0001 0010] [1110 0100] [0000 0000]
  = 0x00 12 e4 00 = 0x0012e400

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- 0x00001402 = [0000 0000] [0000 0000] [0001 0100] [0000 0010]

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  = [0000 0000] [0000 0110] [1010 0100] [0000 0010]

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  = 0x00 06 a4 02 = 0x0006a402

Mechanism: Paging

Limitations of segmentation

> Fragmentation: Inability to use available memory

>> Internal fragmentation: Unused portions internally on each segment

>> External fragmentation: Free segments not usable due to unfit sizes

Limitations of single-level paging

Mechanism: Paging

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Limitations of single-level paging

> Size of page table: E.g., with 32-bit virtual addresses, need a 4MB flat array per process to map a sparse 4GB address space

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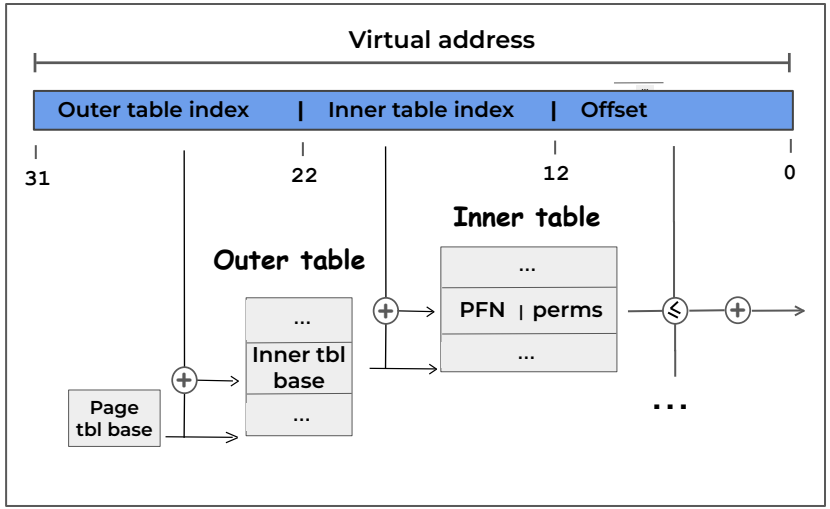
Limitations of single-level paging

> Size of page table: E.g., with 32-bit virtual addresses, need a 4MB flat array per process to map a sparse 4GB address space

> Internal fragmentation: Still an issue, but not as prominent

Mechanism: 2-level hierarchical paging

› Assume 32-bit virtual and physical address space, where the 12 lower bits are for the offset, the 10 middle bits are the index for the inner table, and the 10 higher bits are the index for the outer table



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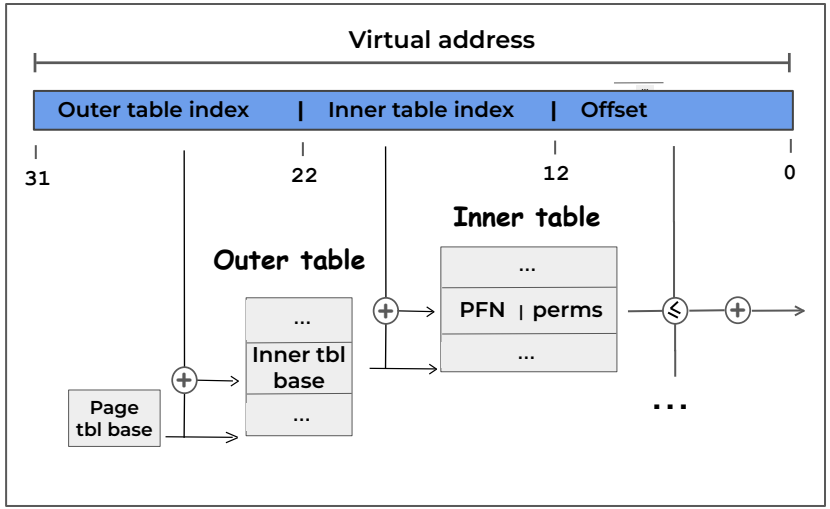

Q: Size of "map-able" address space?

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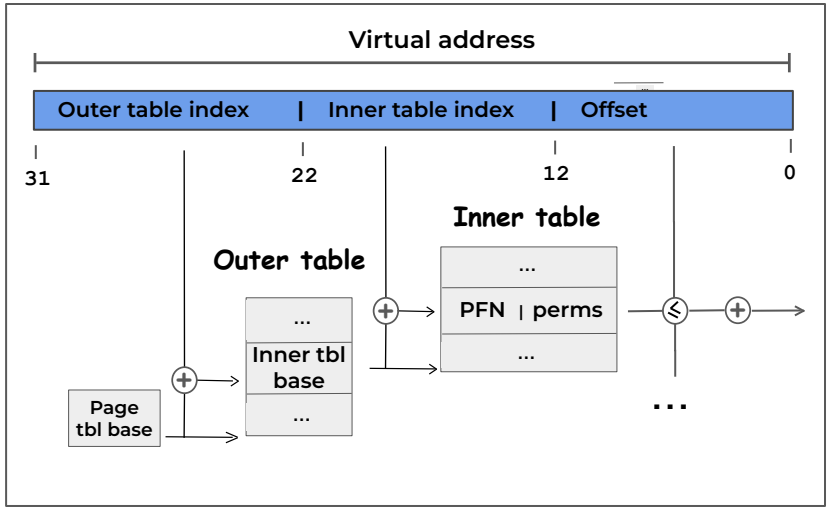

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› **With two pages** (one for each of the outer and inner table): 1 * 1024 PTEs * 4KB = 4MiB

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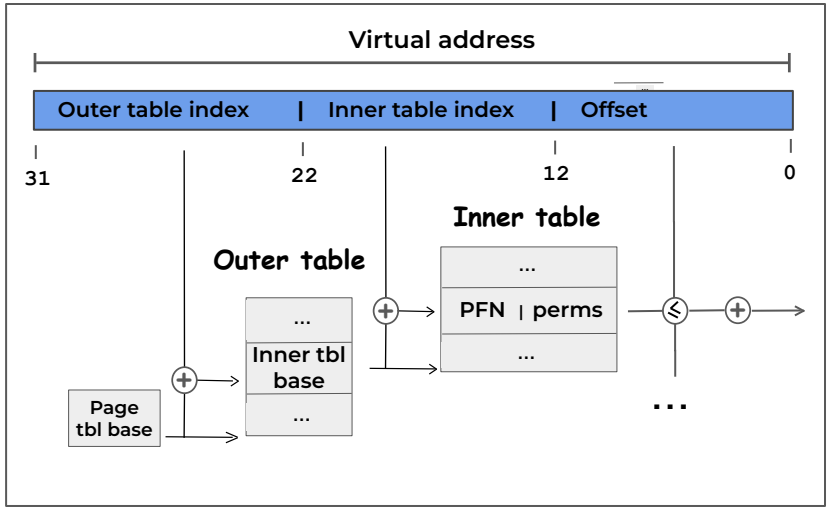

Q: Size of "map-able" address space?

› **With two pages** (one for each of the outer and inner table): 1 * 1024 PTEs * 4KB = 4MiB

› With each additional page in the inner table (i.e., 1024 PTEs), 4 additional MiB can be mapped

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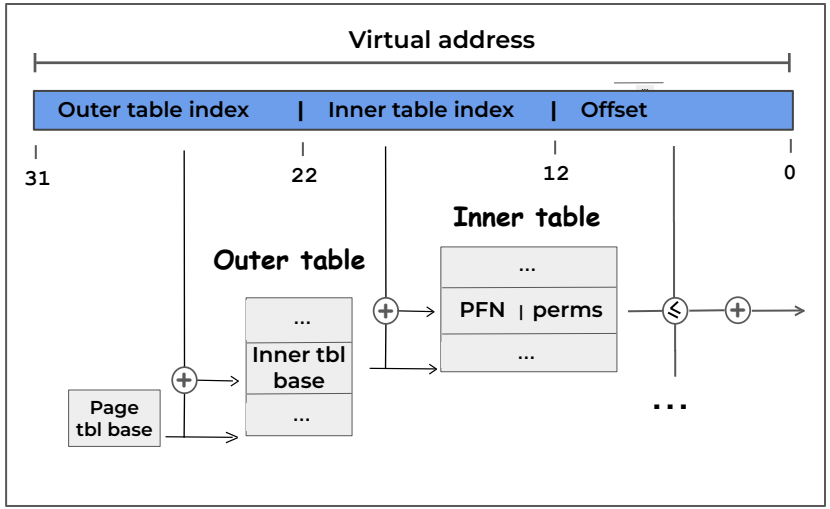

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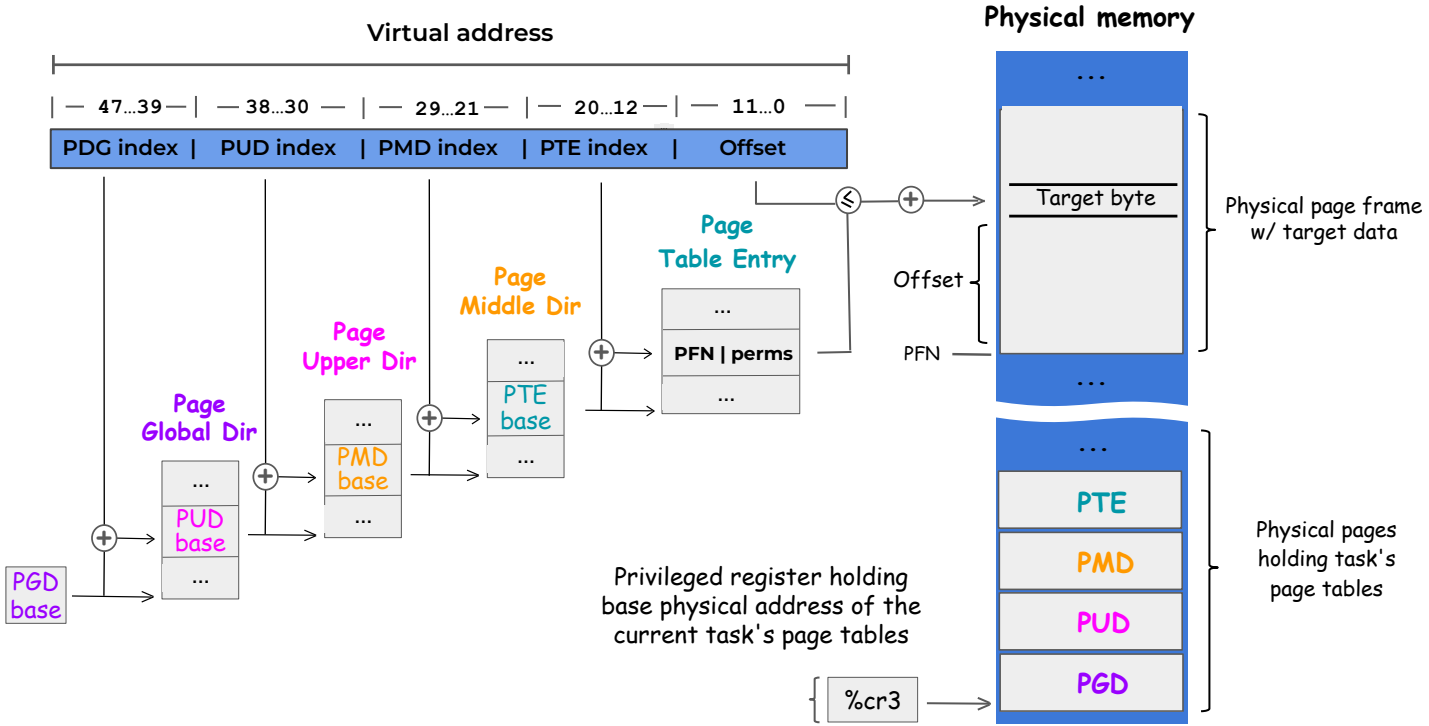
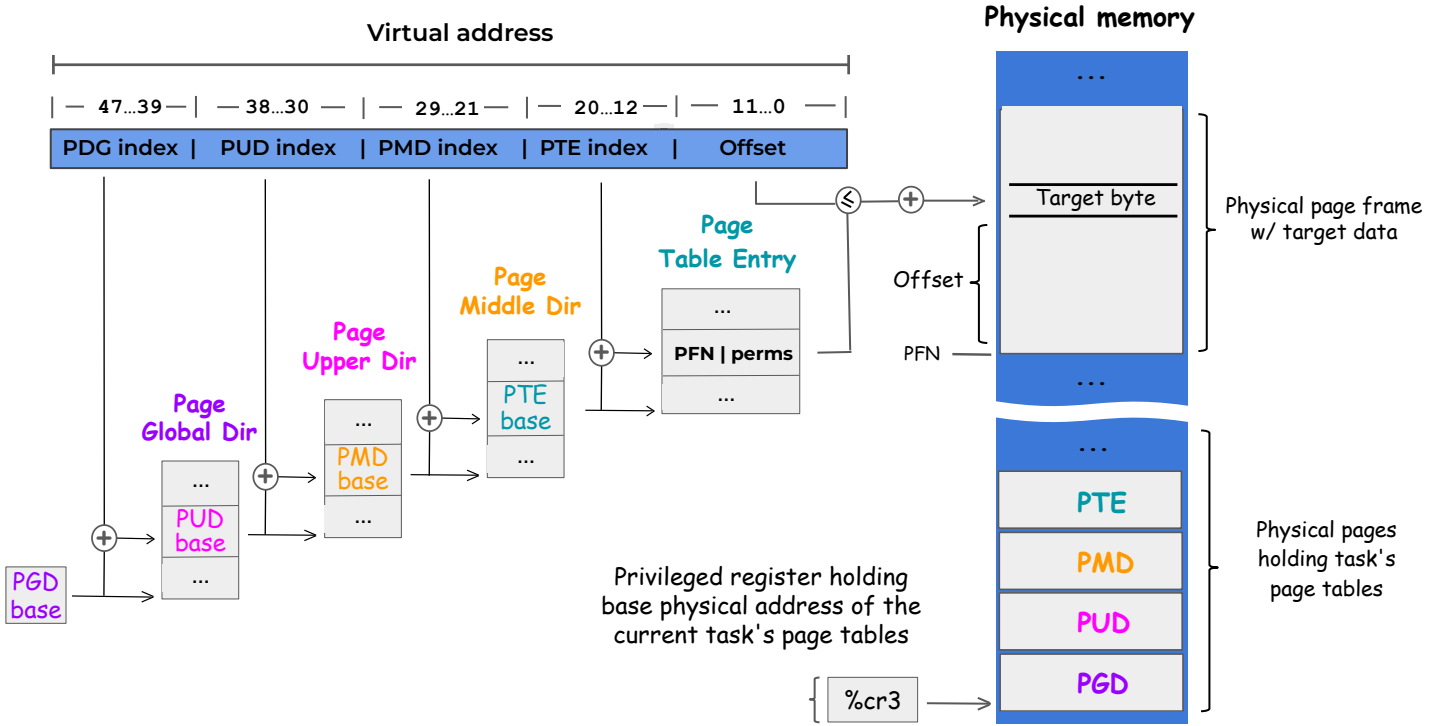
There is another positive side-effect…hang on…

Mechanism: Multi-level paging

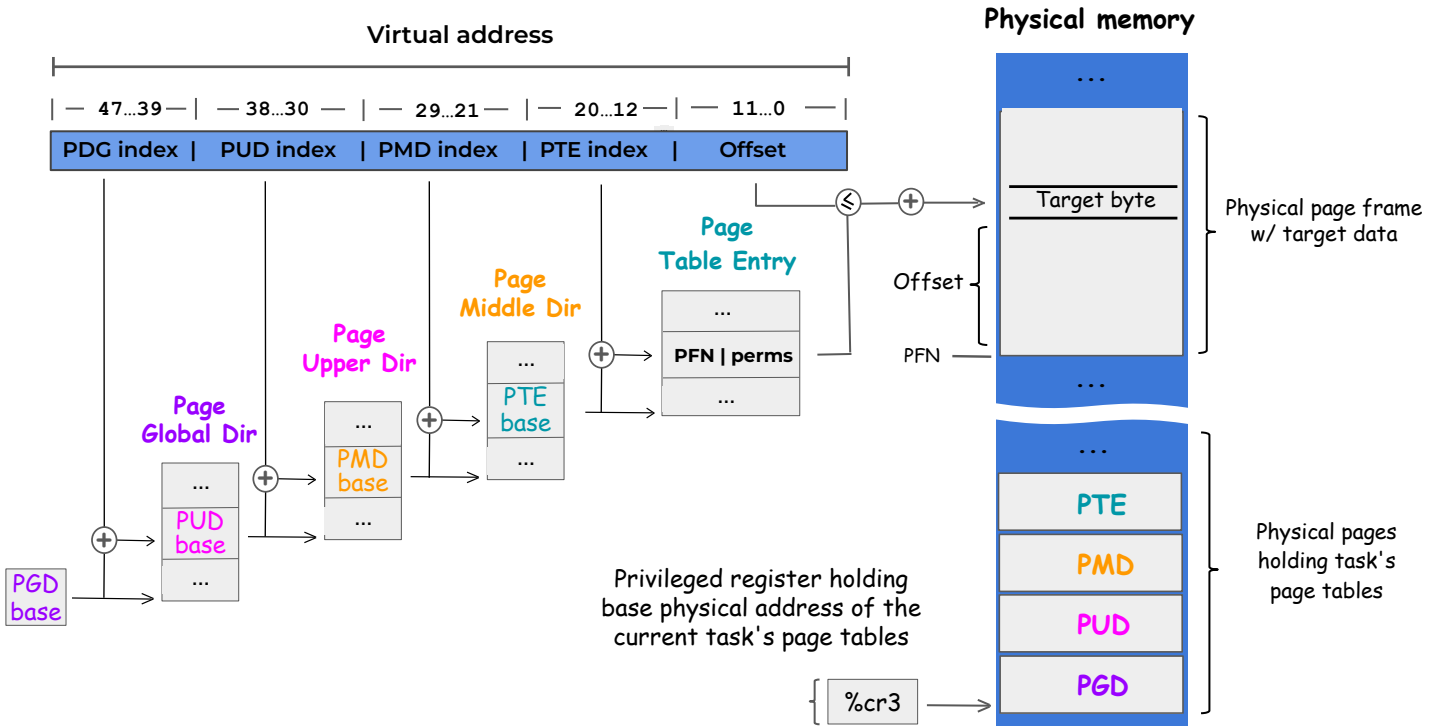


Mechanism: Multi-level paging



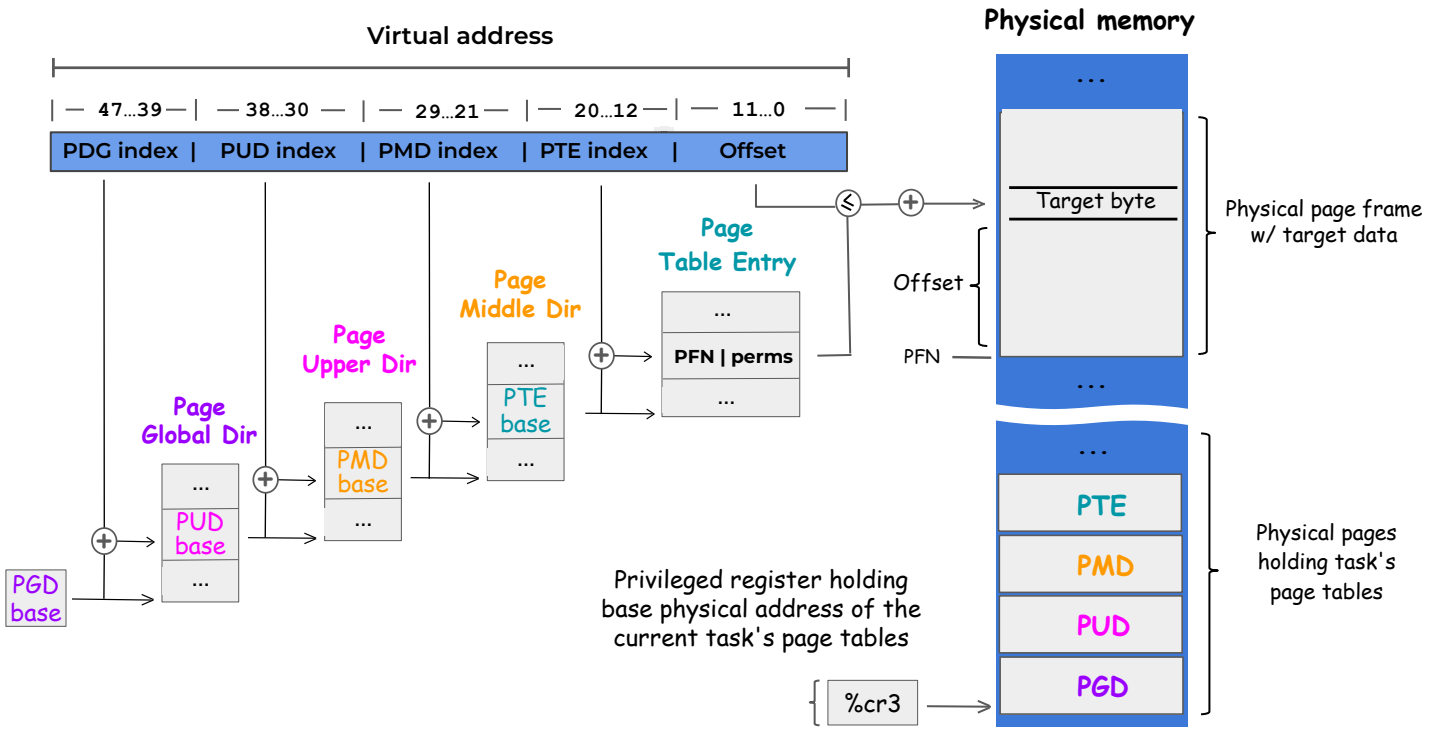
› See relevant linux definitions: here

Mechanism: Multi-level paging



> What is the reach of one page of PTE/PMD/PUD/PGD entries?

Mechanism: Multi-level paging



> What is the reach of one page of PTE/PMD/PUD/PGD entries? **Why care?**

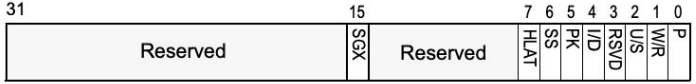
x86 PTE format that maps a 4KB page

63	62–M	M-1	32–12	11–9	8	7	6	5	4	3	2	1	0	
XD	Prot. Key	Ignored	Rsvd.	Address of 4KB page frame	R	Ign.	G	PAT	D	A	PCD	PWT	U/S	R/W	1	PTE: 4KB page
Ignored															0	PTE: not present

0 (P)	Present; must be 1 to map a 4-KByte page
1 (R/W)	Read/write; if 0, writes may not be allowed to the 4-KByte page referenced by this entry (see Section 5.6)
2 (U/S)	User/supervisor; if 0, user-mode accesses are not allowed to the 4-KByte page referenced by this entry (see Section 5.6)
3 (PWT)	Page-level write-through; indirectly determines the memory type used to access the 4-KByte page referenced by this entry (see Section 5.9.2)
4 (PCD)	Page-level cache disable; indirectly determines the memory type used to access the 4-KByte page referenced by this entry (see Section 5.9.2)
5 (A)	Accessed; indicates whether software has accessed the 4-KByte page referenced by this entry (see Section 5.8)
6 (D)	Dirty; indicates whether software has written to the 4-KByte page referenced by this entry (see Section 5.8)

> See Intel Software Developer's Manual

x86 Page fault error codes @%cr2 (faulting addr. @%cr3)



P	0	The fault was caused by a non-present page.
	1	The fault was caused by a page-level protection violation.
W/R	0	The access causing the fault was a read.
	1	The access causing the fault was a write.
U/S	0	A supervisor-mode access caused the fault.
	1	A user-mode access caused the fault.
RSVD	0	The fault was not caused by reserved bit violation.
	1	The fault was caused by a reserved bit set to 1 in some paging-structure entry.
I/D	0	The fault was not caused by an instruction fetch.
	1	The fault was caused by an instruction fetch.
PK	0	The fault was not caused by protection keys.
	1	There was a protection-key violation.
SS	0	The fault was not caused by a shadow-stack access.
	1	The fault was caused by a shadow-stack access.
HLAT	0	The fault occurred during ordinary paging or due to access rights.
	1	The fault occurred during HLAT paging.
SGX	0	The fault is not related to SGX.
	1	The fault resulted from violation of SGX-specific access-control requirements.

> See Intel Software Developer's Manual

Checking the address space size of your machine

Checking the address space size of your machine

```
→  ~ cat /proc/$$/maps | head
aaaaab8d0000-aaaaab9a3000 r-xp 00000000 08:02 2375001
aaaaab9b3000-aaaaab9b5000 r--p 000d3000 08:02 2375001
aaaaab9b5000-aaaaab9bb000 rw-p 000d5000 08:02 2375001
aaaaab9bb000-aaaaab9cf000 rw-p 00000000 00:00 0
aaaaac024000-aaaaac40b000 rw-p 00000000 00:00 0
ffffb82b0000-ffffb8530000 r--s 00000000 08:02 2890570
ffffb8530000-ffffb853f000 r-xp 00000000 08:02 2495184
ffffb853f000-ffffb854e000 ---p 0000f000 08:02 2495184
ffffb854e000-ffffb854f000 r--p 0000e000 08:02 2495184
ffffb854f000-ffffb8550000 rw-p 0000f000 08:02 2495184
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aaaaab9bb000-aaaaab9cf000 rw-p 00000000 00:00 0
aaaaac024000-aaaaac40b000 rw-p 00000000 00:00 0
ffffb82b0000-ffffb8530000 r--s 00000000 08:02 2890570
ffffb8530000-ffffb853f000 r-xp 00000000 08:02 2495184
ffffb853f000-ffffb854e000 ---p 0000f000 08:02 2495184
ffffb854e000-ffffb854f000 r--p 0000e000 08:02 2495184
ffffb854f000-ffffb8550000 rw-p 0000f000 08:02 2495184
```

- Why am I seeing 12 hexadecimal digits?

Checking the address space size of your machine

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aaaaab9b3000-aaaaab9b5000 r--p 000d3000 08:02 2375001
aaaaab9b5000-aaaaab9bb000 rw-p 000d5000 08:02 2375001
aaaaab9bb000-aaaaab9cf000 rw-p 00000000 00:00 0
aaaaac024000-aaaaac40b000 rw-p 00000000 00:00 0
ffffb82b0000-ffffb8530000 r--s 00000000 08:02 2890570
ffffb8530000-ffffb853f000 r-xp 00000000 08:02 2495184
ffffb853f000-ffffb854e000 ---p 0000f000 08:02 2495184
ffffb854e000-ffffb854f000 r--p 0000e000 08:02 2495184
ffffb854f000-ffffb8550000 rw-p 0000f000 08:02 2495184
→  ~ cat /boot/config-`uname -r` | grep "VA_BITS\|PA_BITS"
# CONFIG_ARM64_VA_BITS_39 is not set
CONFIG_ARM64_VA_BITS_48=y
CONFIG_ARM64_VA_BITS=48
CONFIG_ARM64_PA_BITS_48=y
CONFIG_ARM64_PA_BITS=48
```

How is virtual memory implemented?

> Usually considered the most complex kernel subsystem

- It's simple if you view it as an index

Ask the right questions

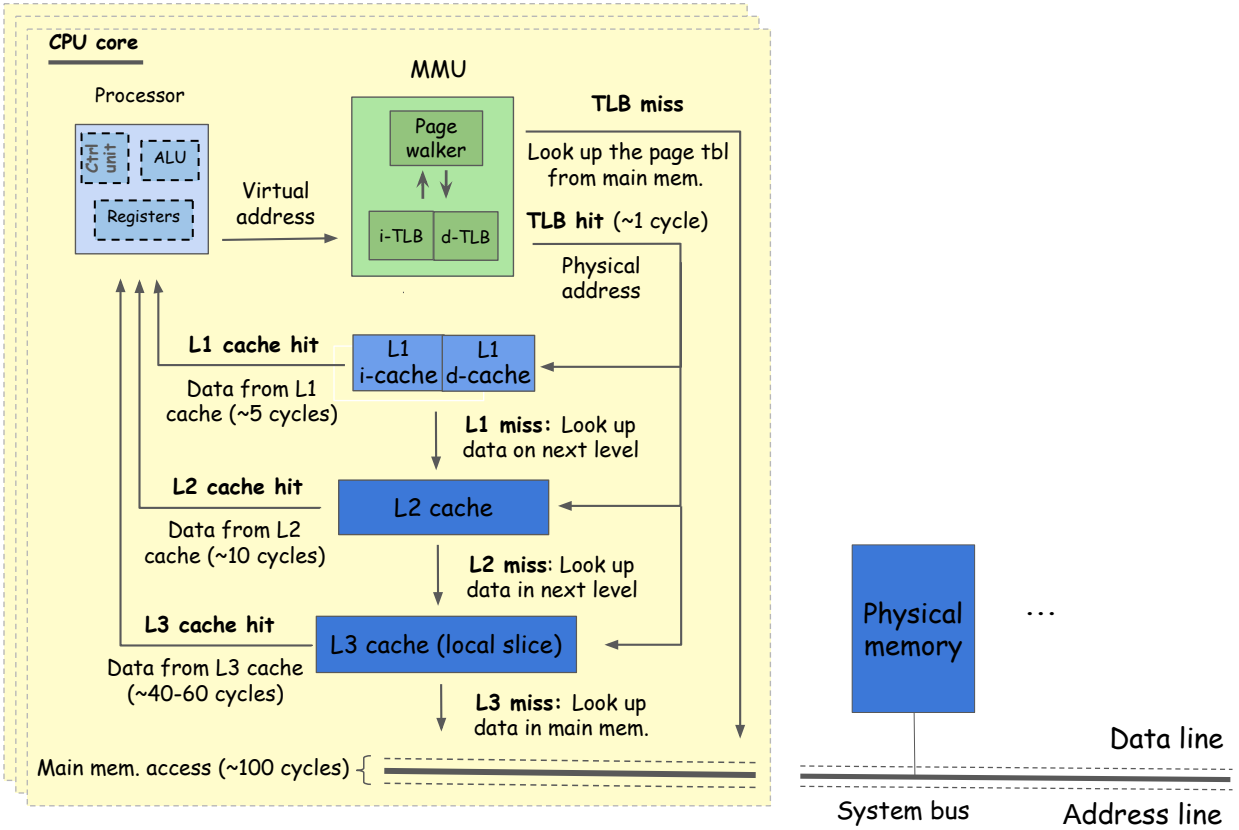
~~Q1: What are the entries of the index?~~

Q2: How are the entries of the index used?

~~Q3: How are the entries of the index allocated?~~

Q4: How are the entries of the index replaced?

Translation Lookaside Buffer (TLB)



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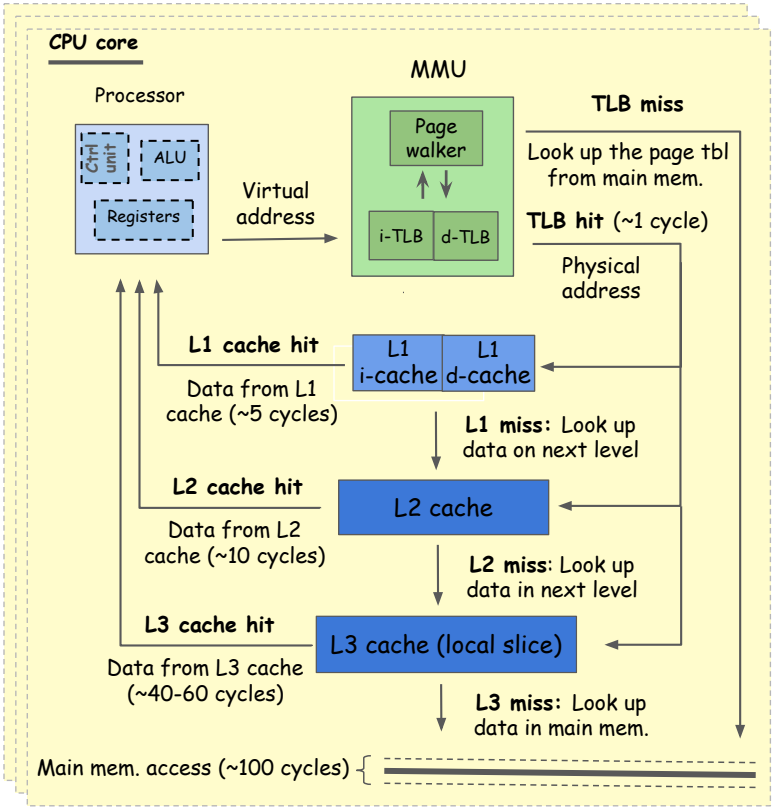
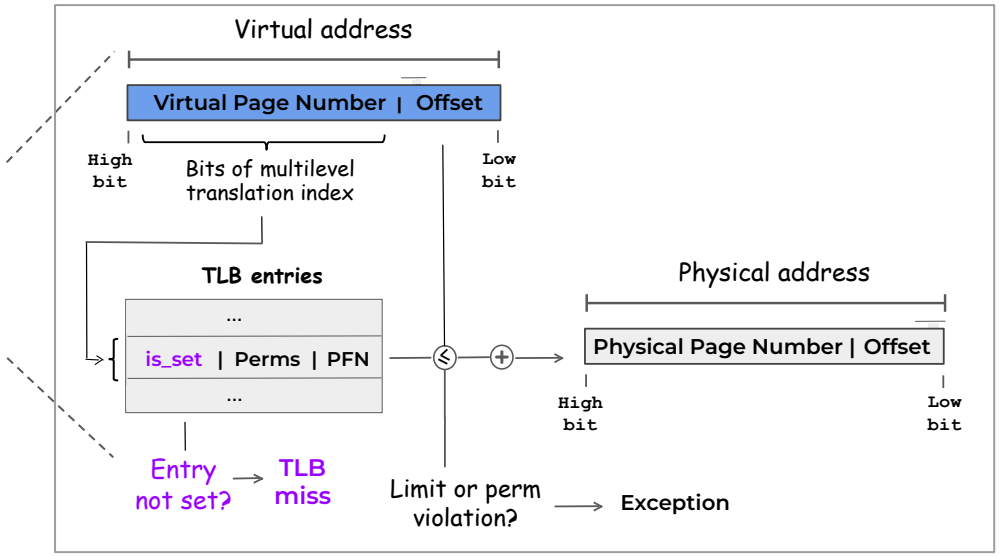
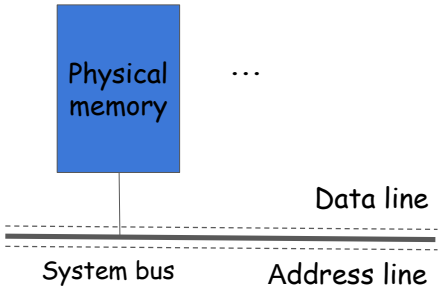
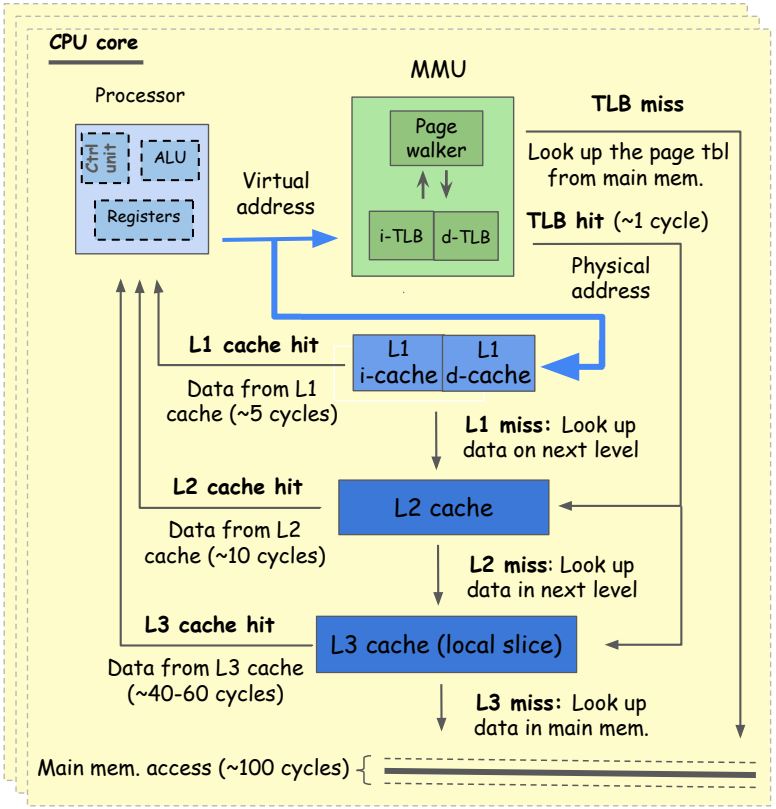






L1 cache: Why not virtually indexed and tagged?

L1 cache: Why not virtually indexed and tagged?



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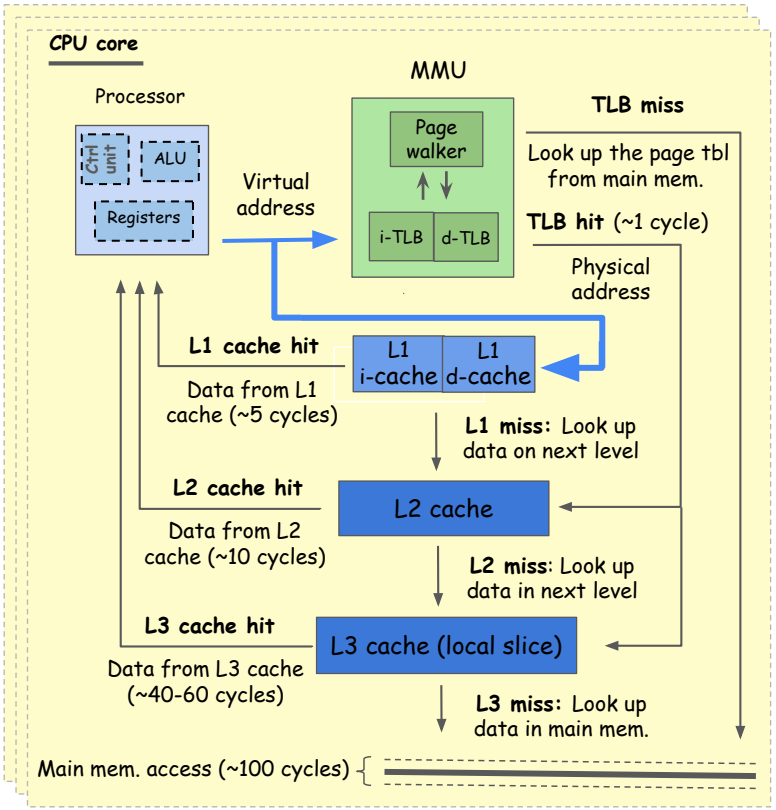

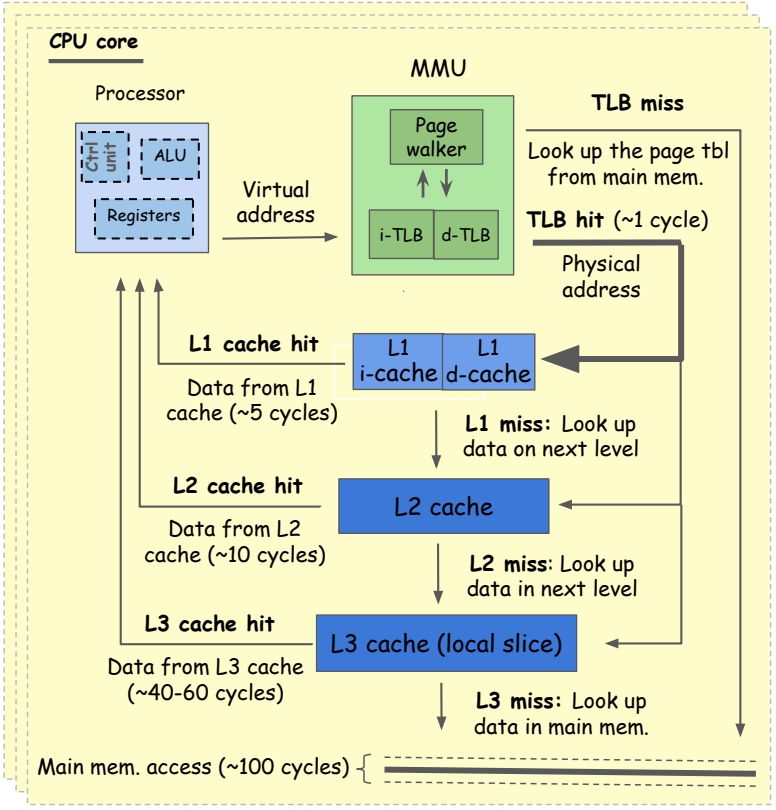

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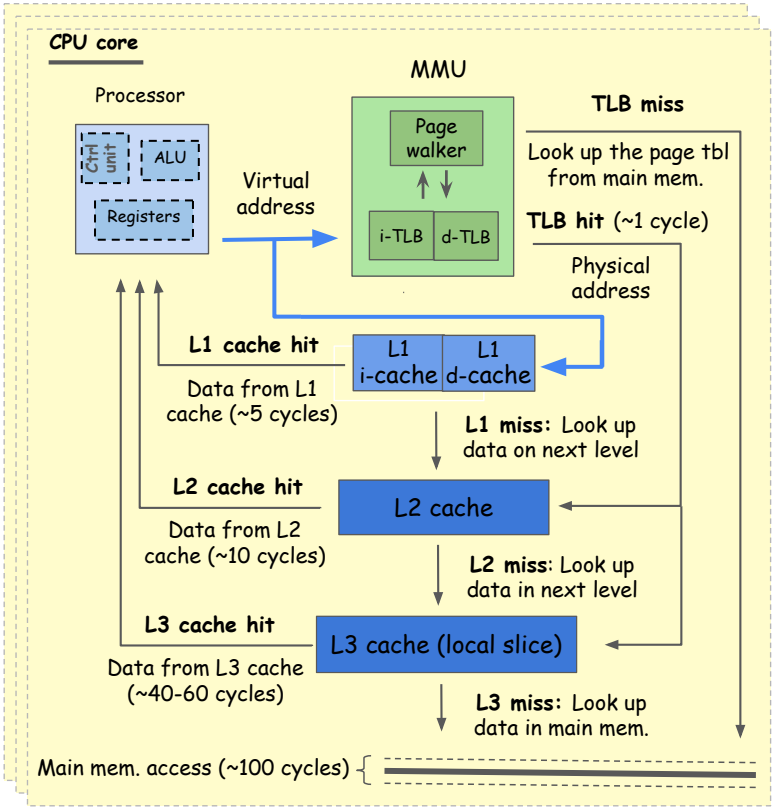

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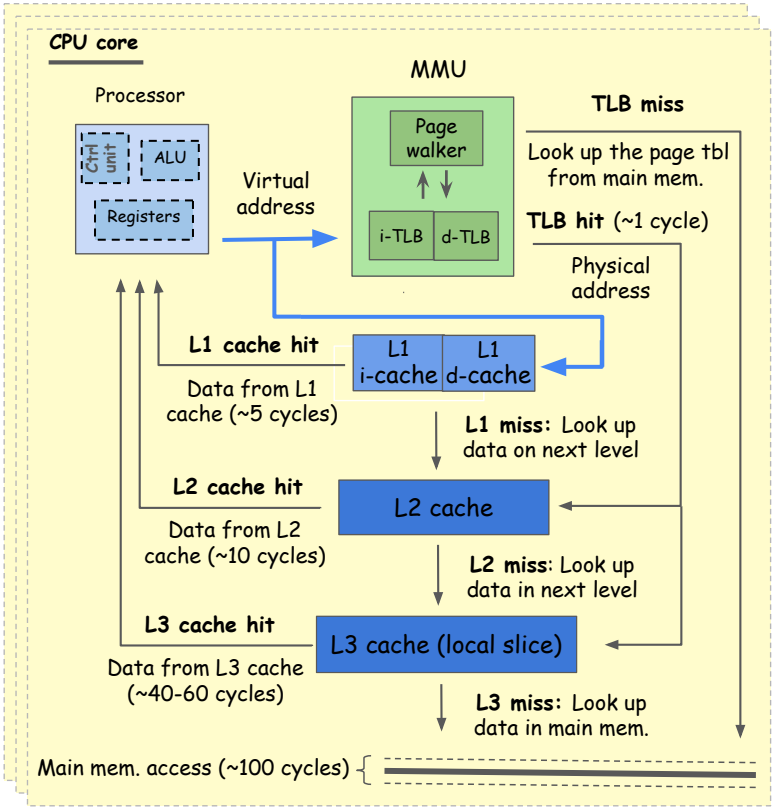

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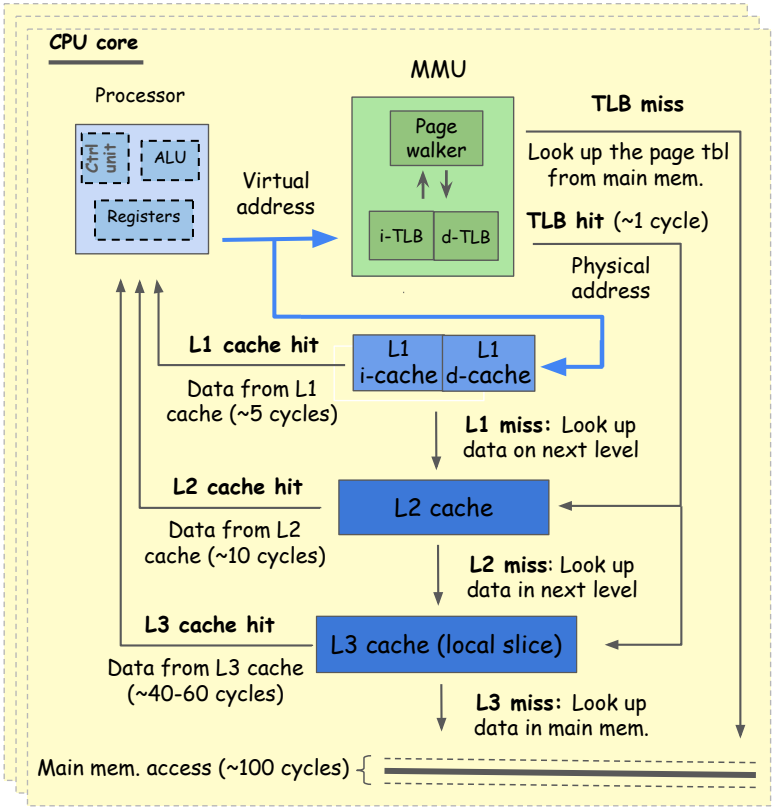

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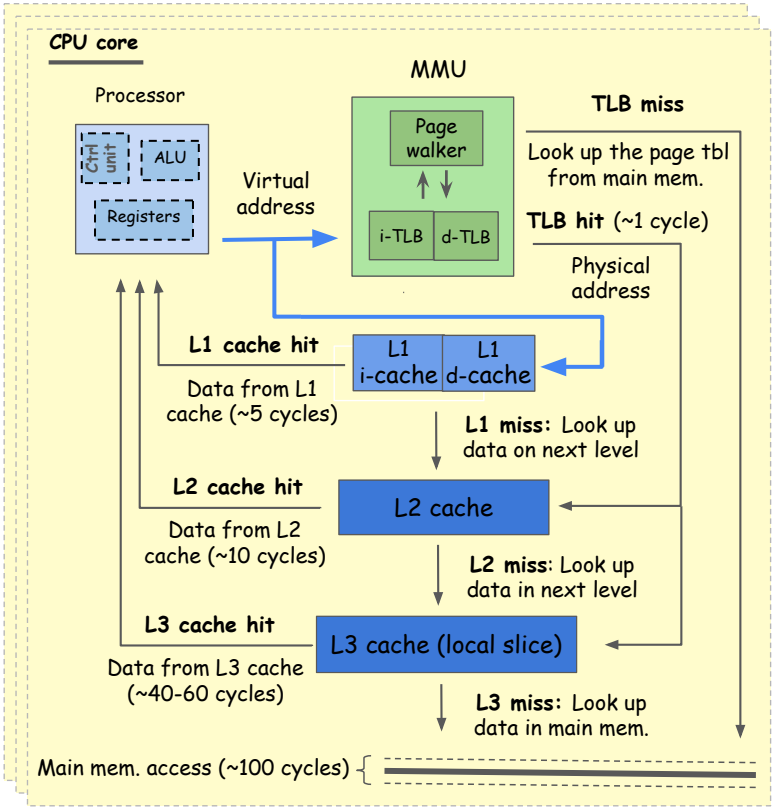

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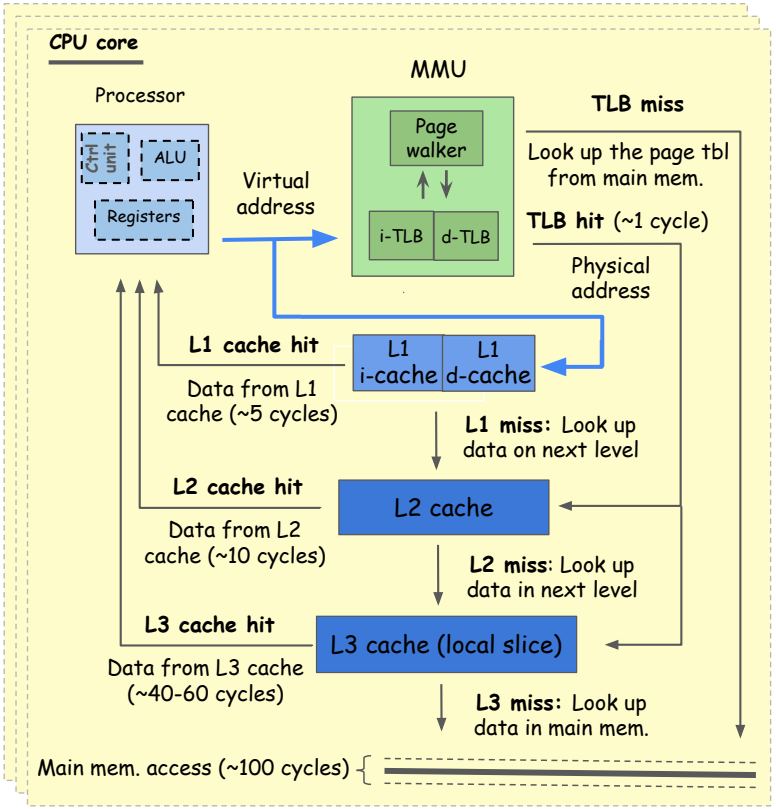

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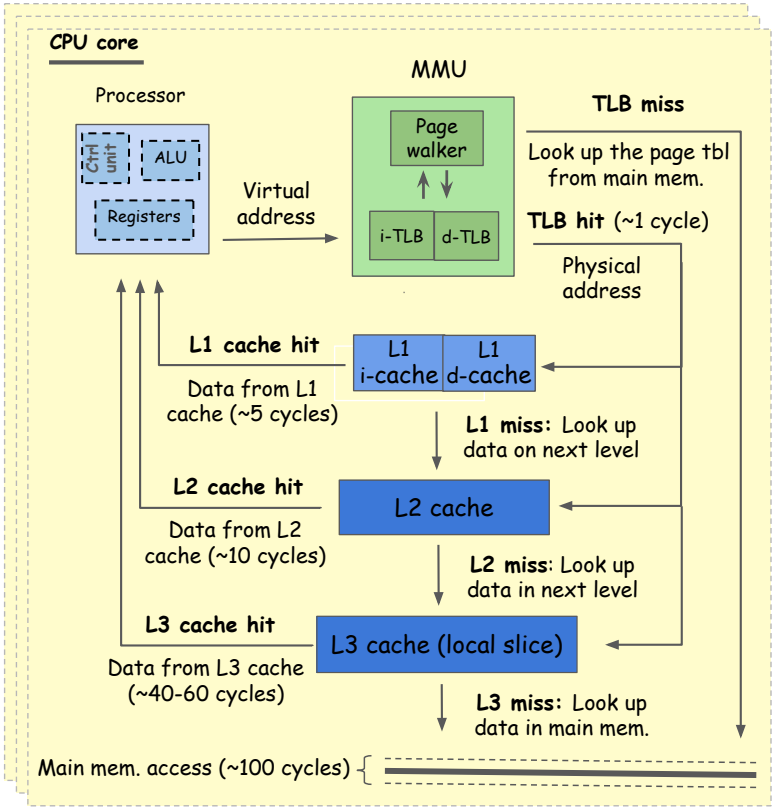
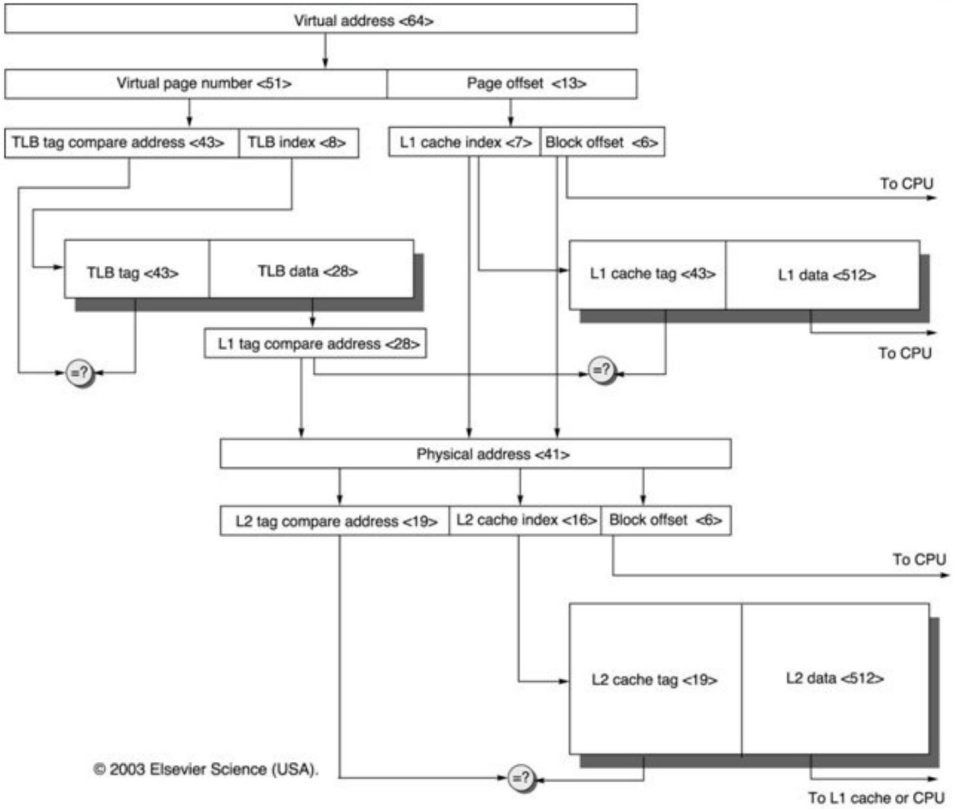
>> Page coloring (beyond scope)

>> Use VIPT or PIPT caches

L1 cache: Virtually-indexed / Physically-tagged





How is virtual memory implemented?

- **Usually considered the most complex kernel subsystem**
- It's simple if you view it as an index

Ask the right questions

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The working set model for program behavior

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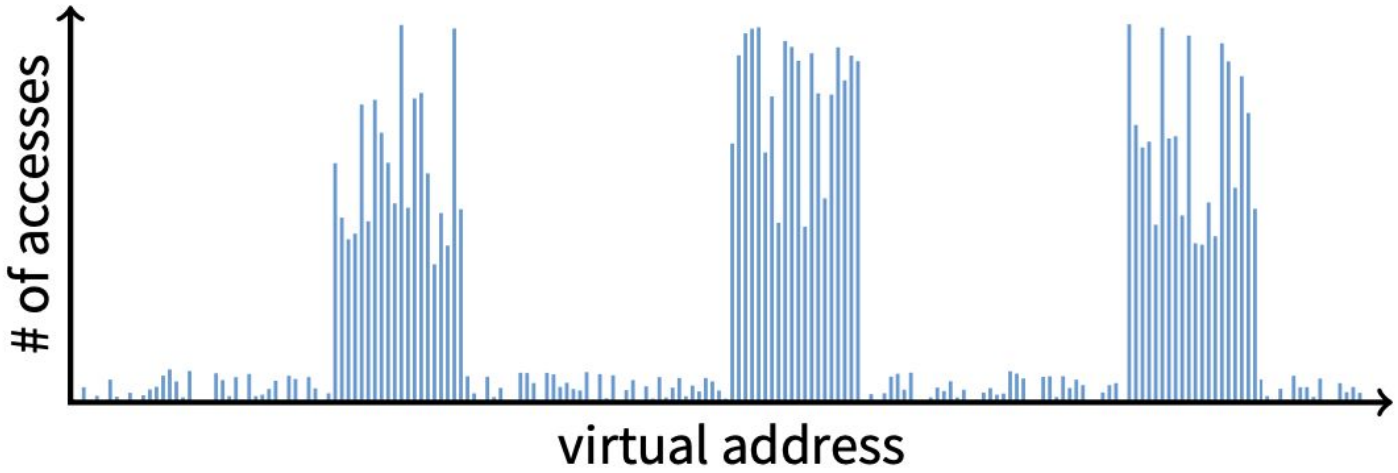

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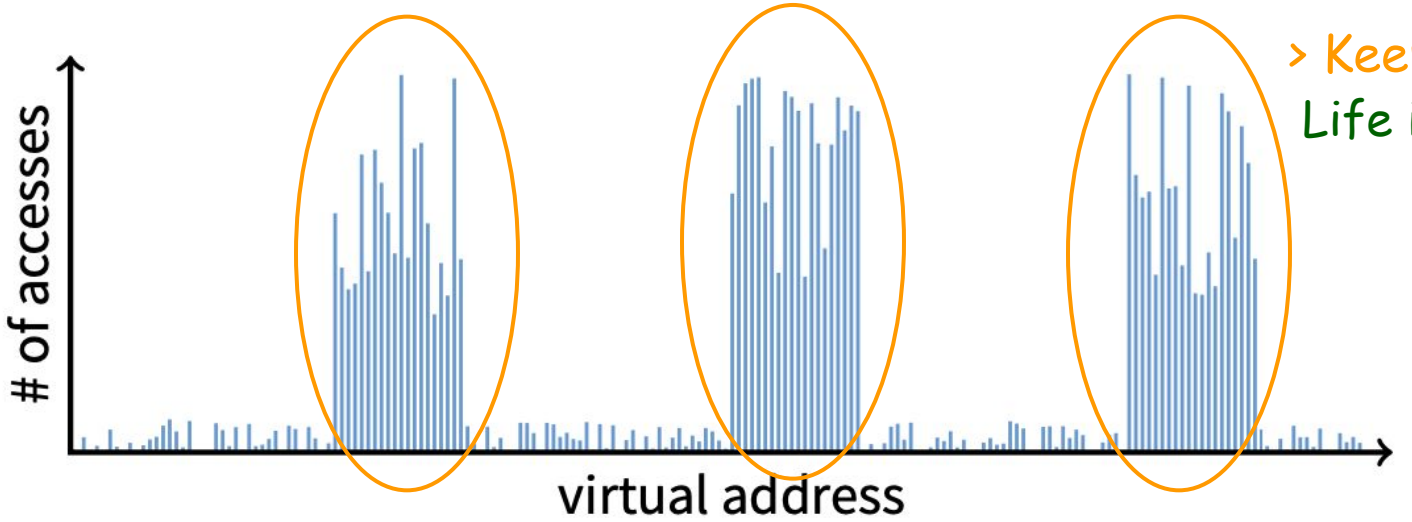
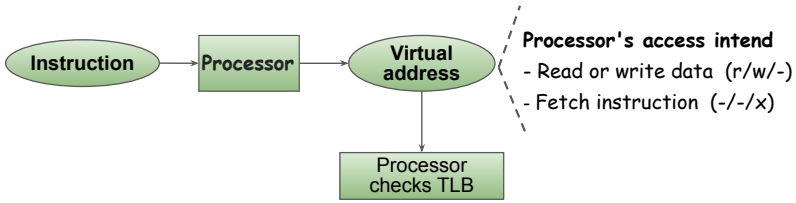


> Keep these "hot"?
Life is good...

Demand paging via page fault handling



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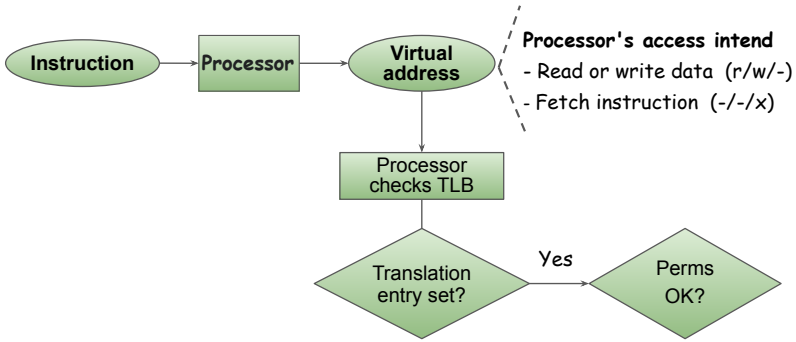

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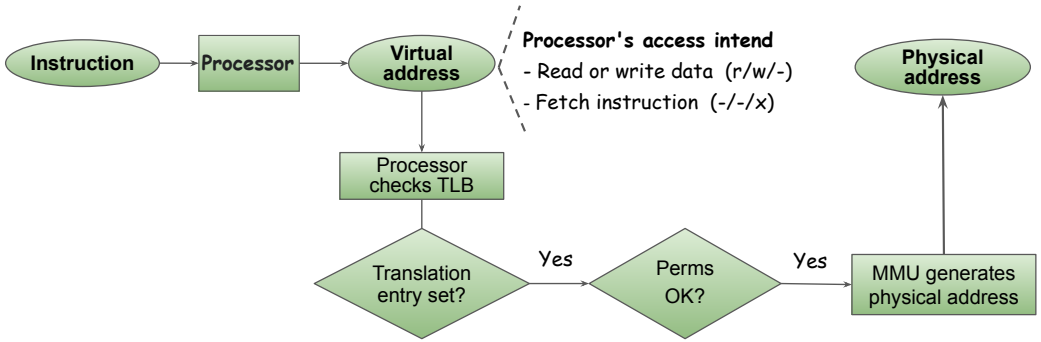

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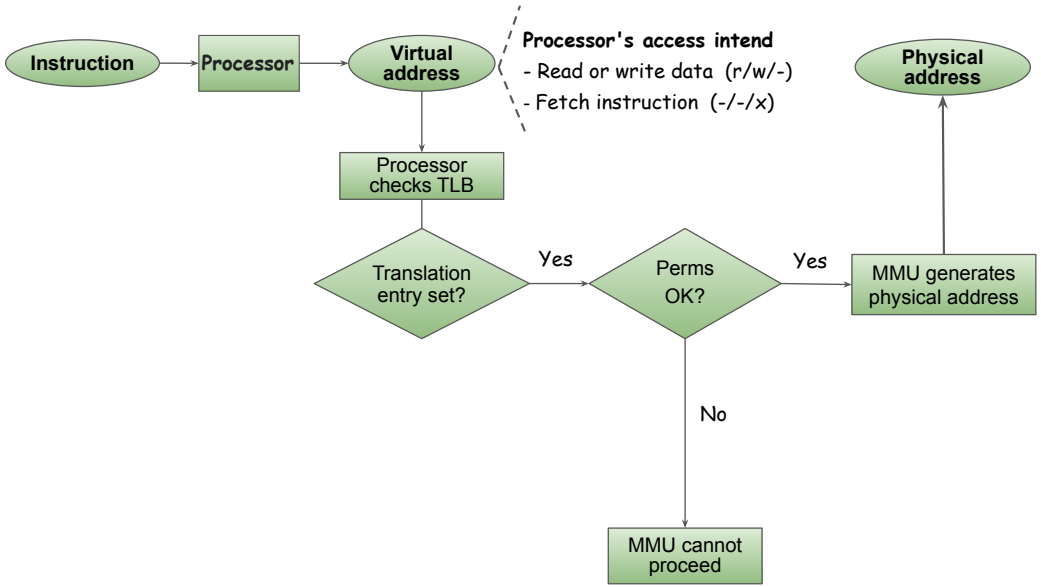

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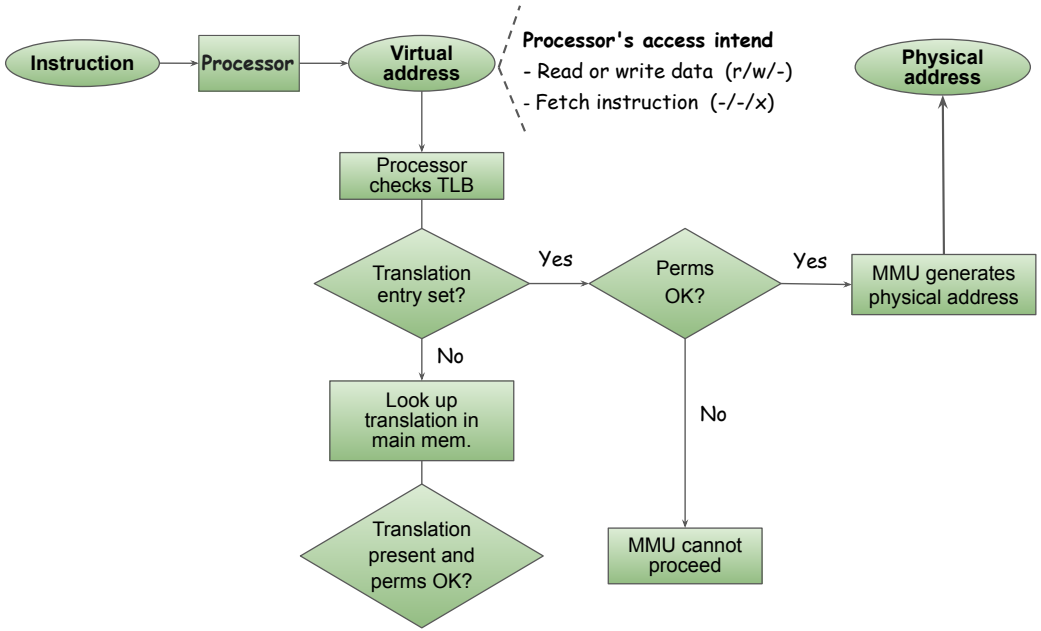

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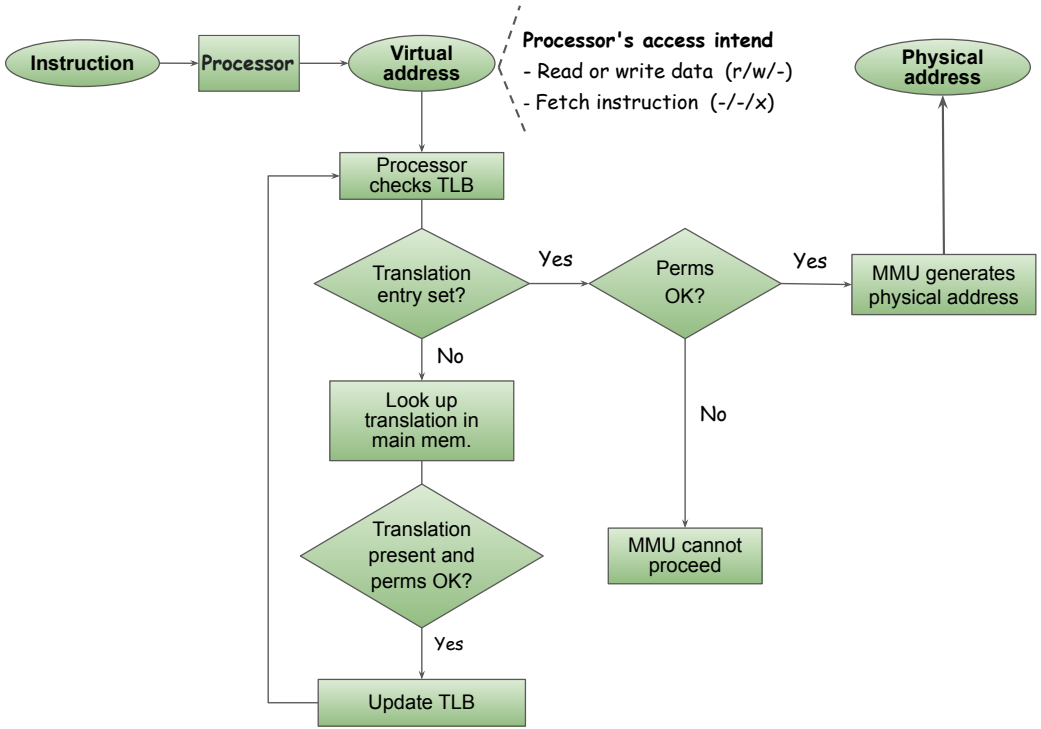

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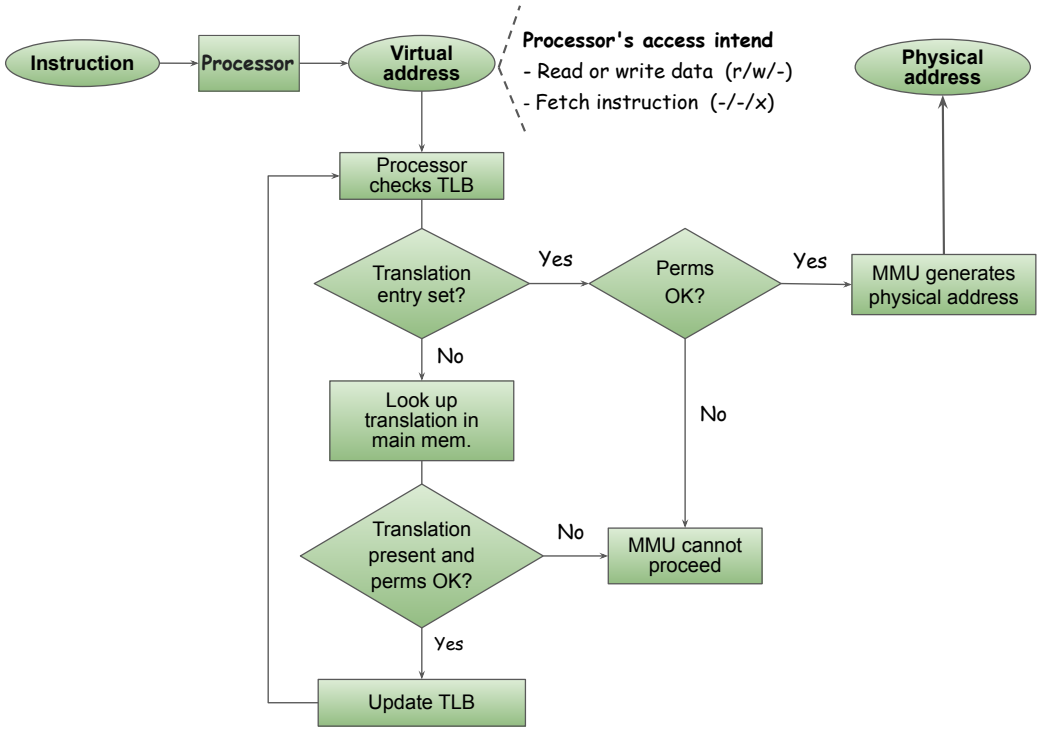

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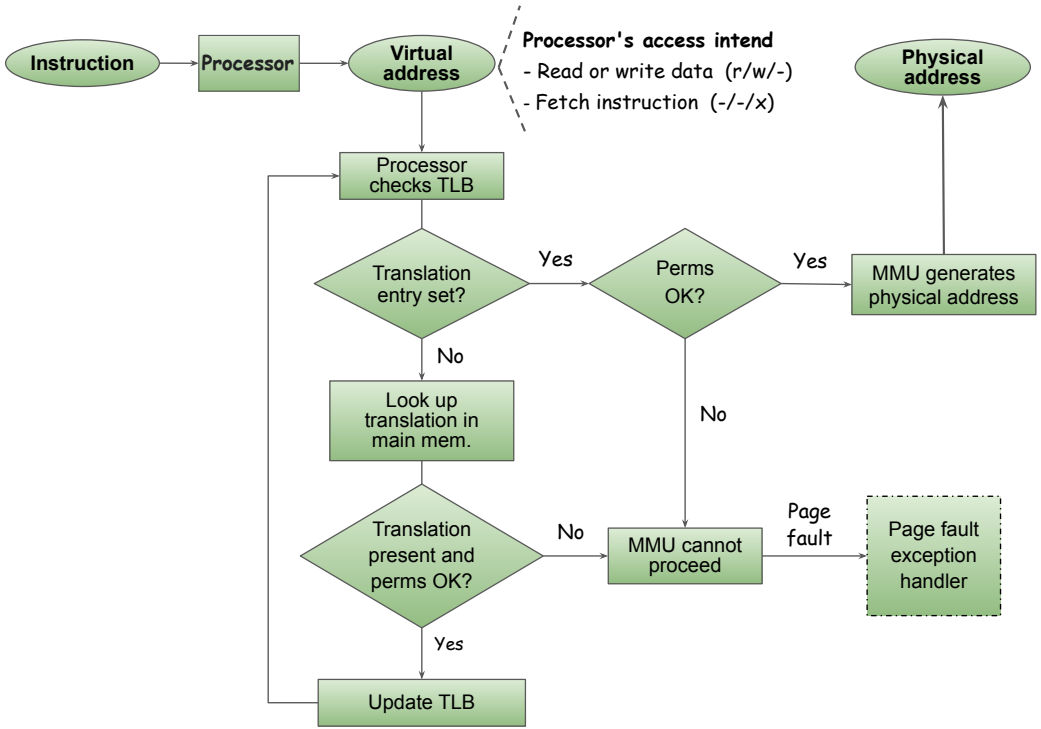

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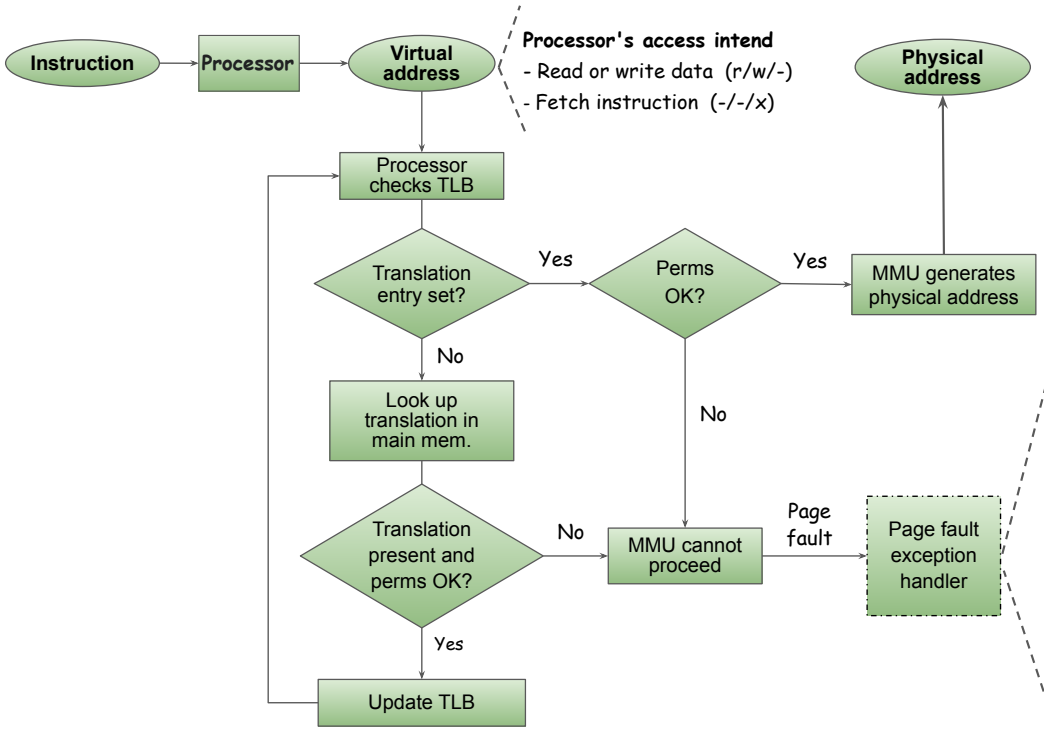

Page fault handling (see here and here)

> Access **not** permitted (see here) => SIGSEGV

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>>> File-backed VMA (see here)

Minor p.f. => do_read_fault

=> do_cow_fault

=> do_shared_fault

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Minor p.f => do_anonymous_page

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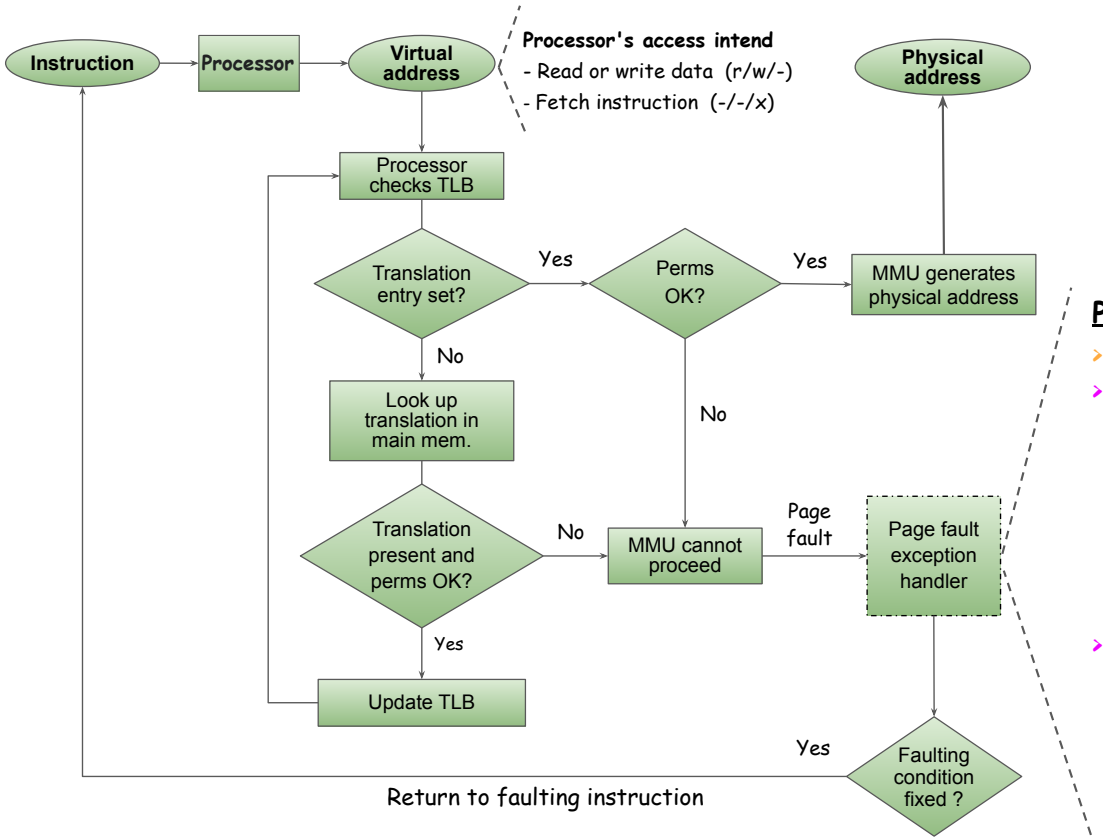

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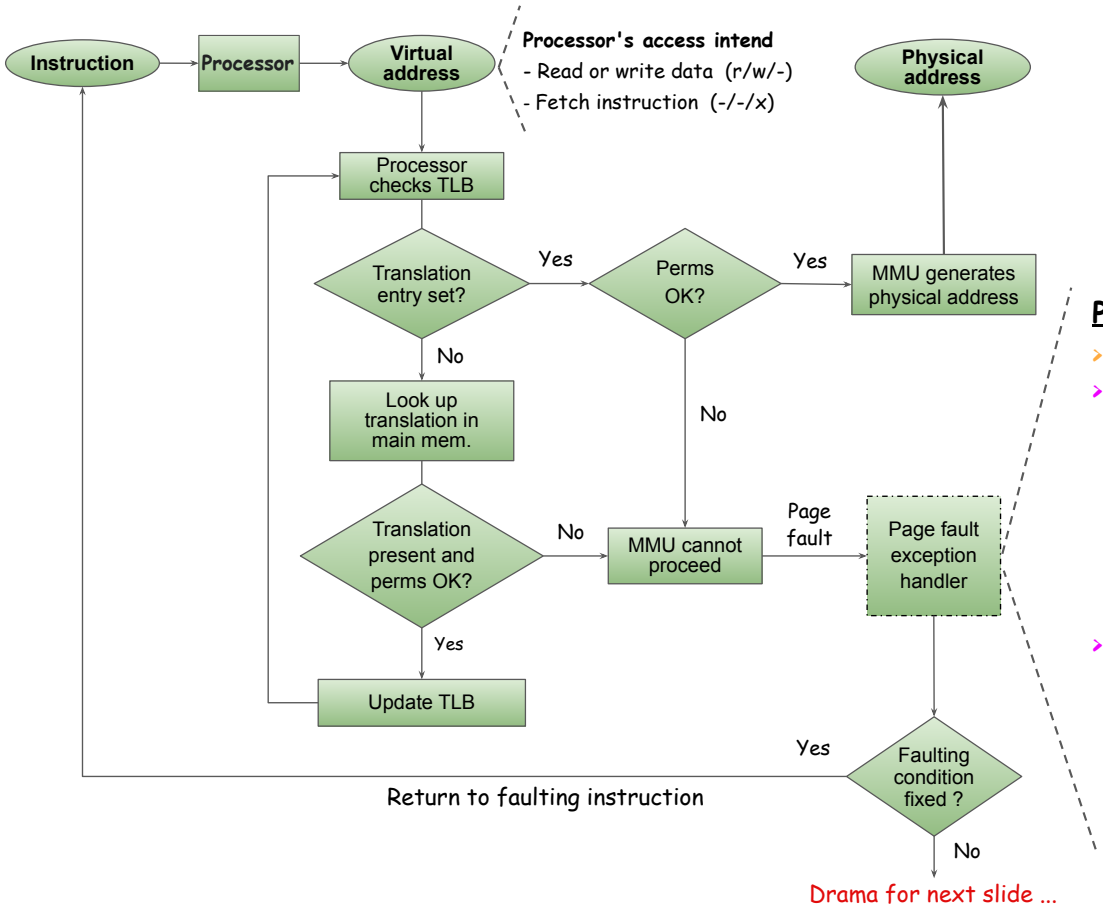

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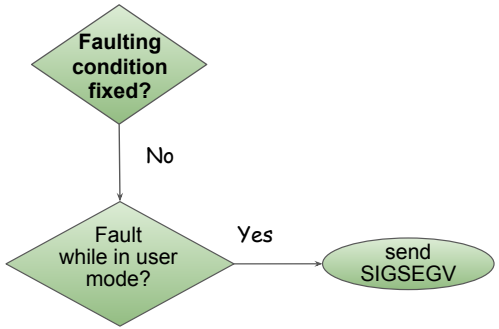

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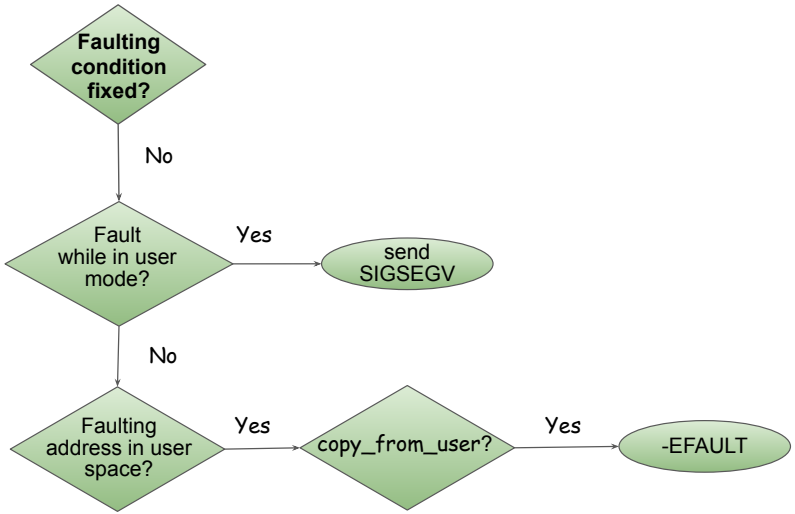

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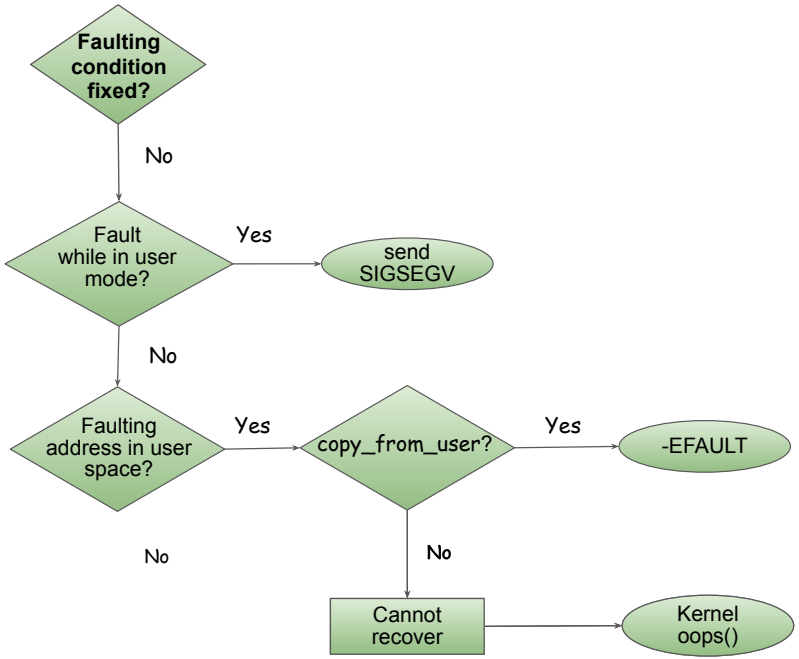

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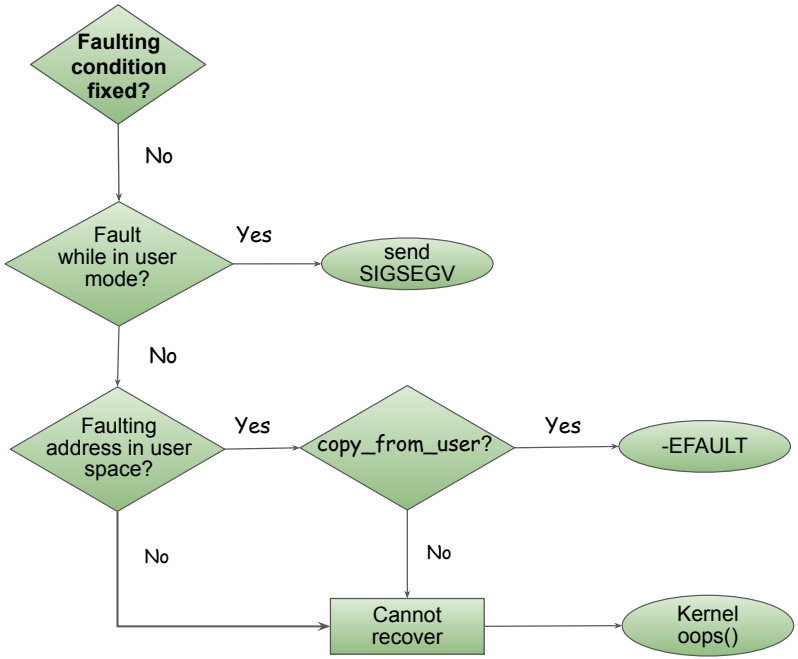

Page fault demo: read->write vs. write->read

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  char a;
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  for (int i = 0; i < vma_size; i += 4096) {
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Read pg faults

Write pg faults

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Read pg faults

Write pg faults

Write pg faults

No read pg faults

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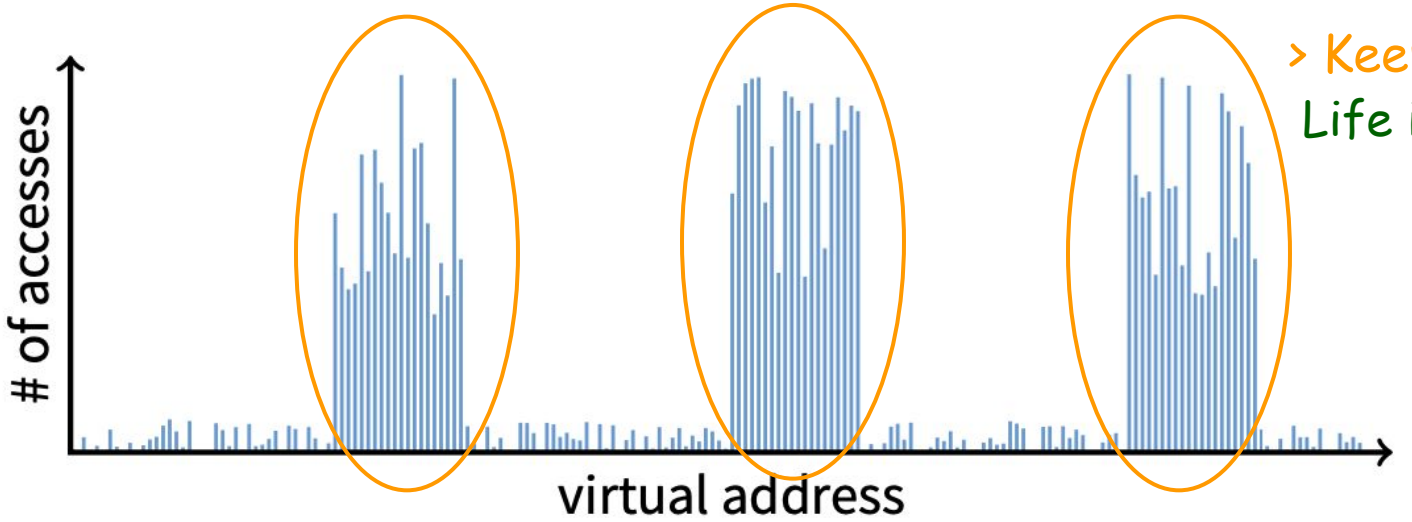
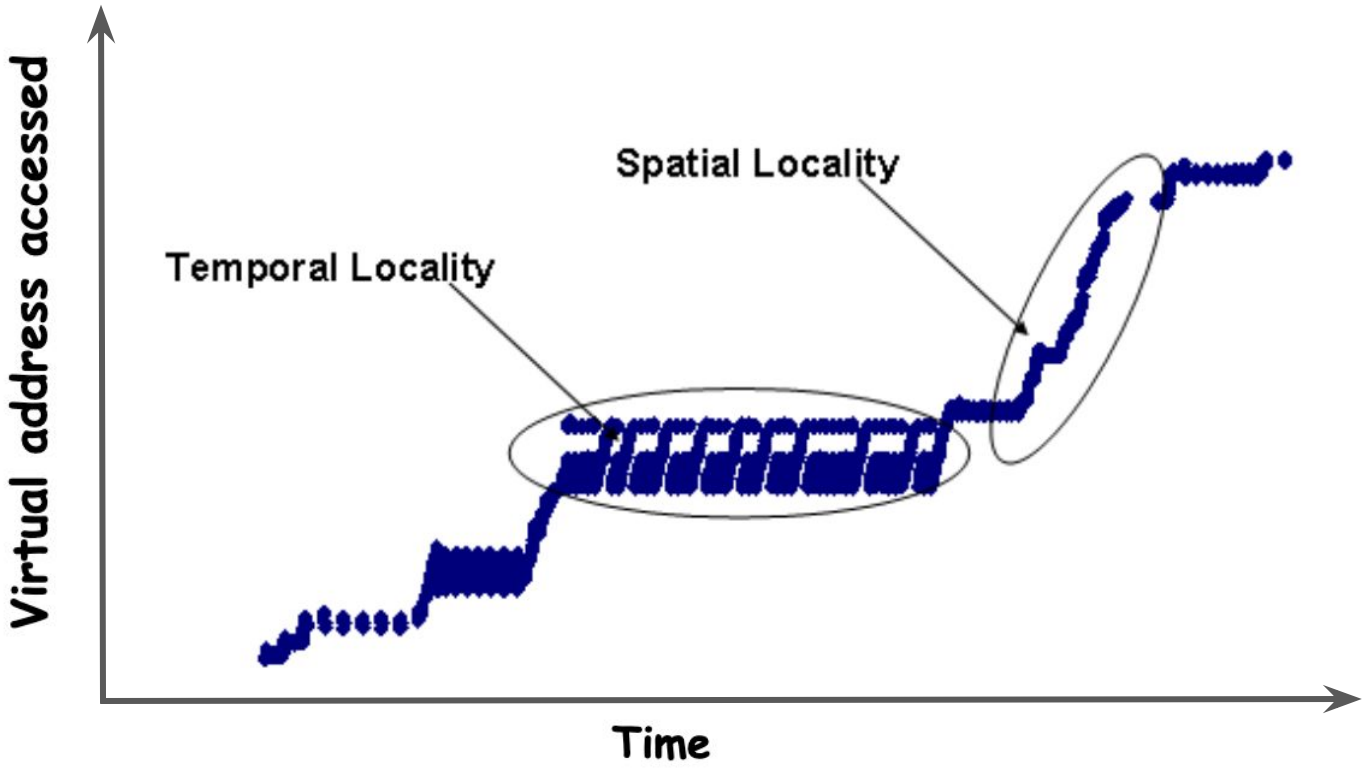


> Keep these "hot"?
Life is good...

Temporal and spatial locality



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- Translation entries w/ "accessed" bits off => Not recently accessed

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- Last resort: Out-Of-Memory (OOM) killer terminates the process

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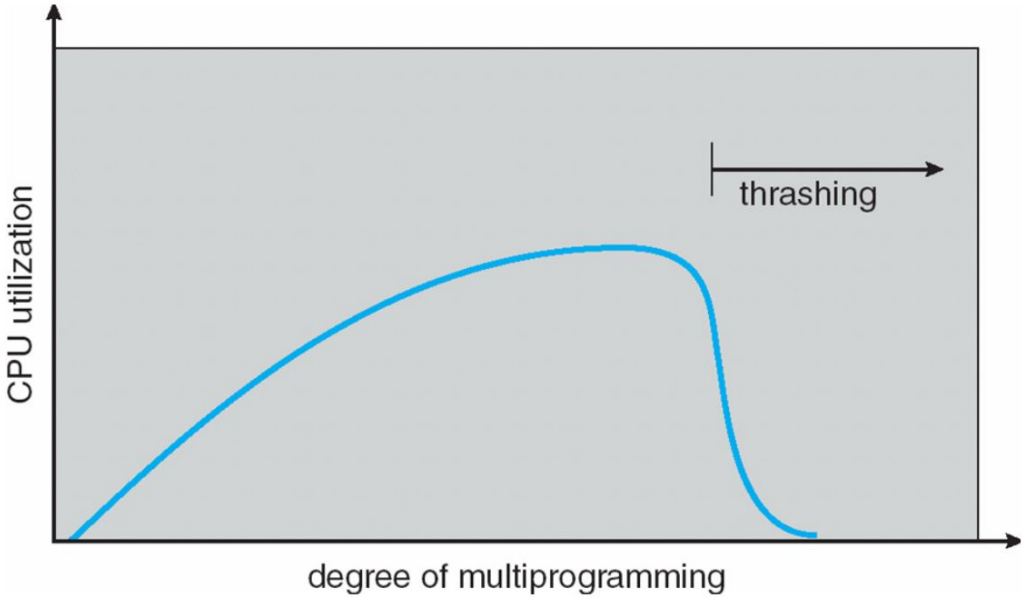

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POSIX Memory management syscalls (cont'ed)

void *mmap (void *addr, ...)

> Creates a new mapping in the virtual address space of the calling process

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int mprotect (void *addr, size_t len, int prot)

> Updates the protections for page(s) in range [addr, addr+len) to "prot"

- addr: Must be aligned to a page boundary
- On success, mprotect(...) returns 0

POSIX Memory management syscalls (cont'ed)

int msync (void *addr, ...):

> Flushes to disk changes made to the in-kernel copy of a file that was mapped into memory using mmap

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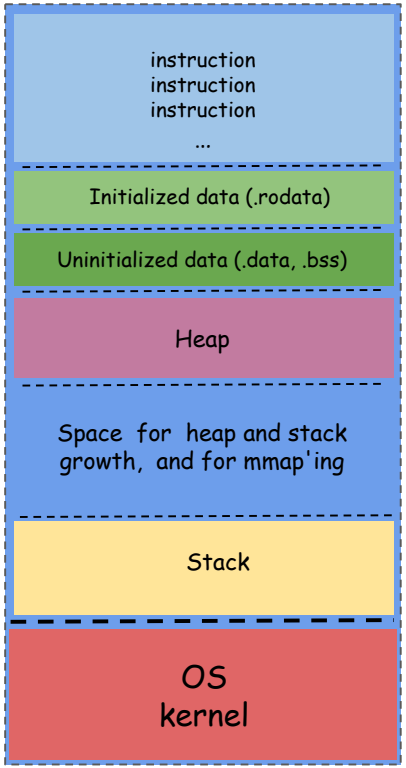
void *mlock/unlock (void *addr, ...)

> Locks/unlocks part or all of the calling process's virtual address space into main mem. preventing that memory from being paged to the swap area

- On success, mlock(...)/unlock(...) returns 0

Putting it all together: 1) Per-process index of VAS segments



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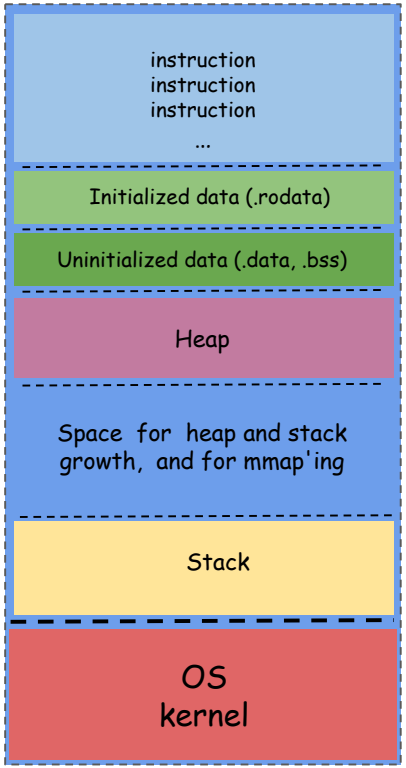


```
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    char comm[TASK_COMM_LEN];
    struct mm_struct *active_mm;
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        ...
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        unsigned long start_code, end_code;
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        unsigned long start_stack;
        struct maple_tree mm_mt;
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› Mapple tree: Read here

```
➜ git:(master) ✗  cat /proc/12453/maps
aaaadcda0000-aaaadcda1000 r-xp  ... /foo
aaaadcdb0000-aaaadcdb1000 r--p  ... /foo
aaaadcdb1000-aaaadcdb2000 rw-p ... /foo
...
aaaaed20d000-aaaaed22e000 rw-p ... [heap]
ffffbe610000-ffffbe798000 r-xp ... libc.so
ffffbe798000-ffffbe7a7000 ---p ... libc.so
...
fffff6461000-fffff6482000 rw-p ... [stack]
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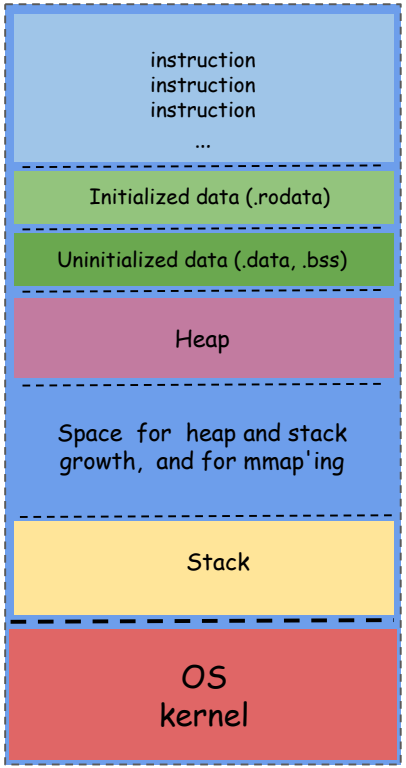
Putting it all together: (1/3) Per-process index of VAS segments

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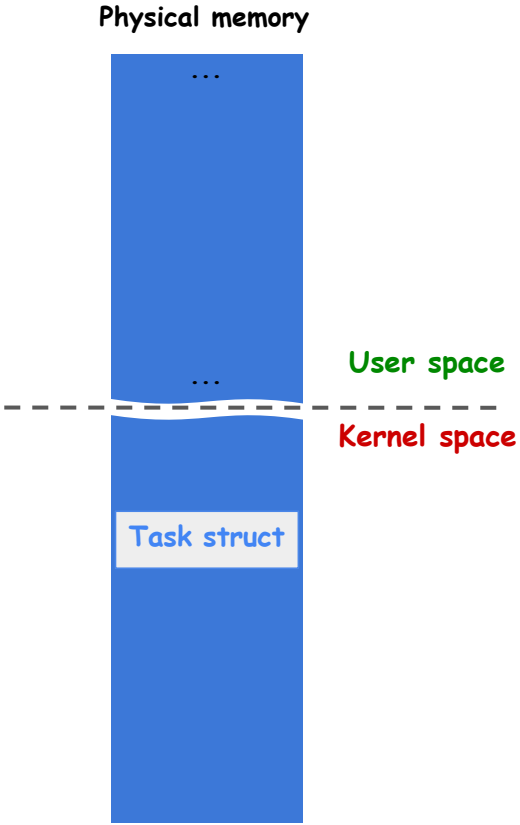

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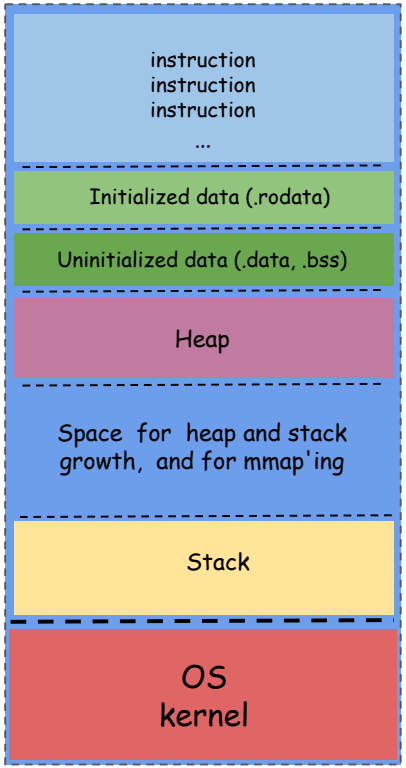

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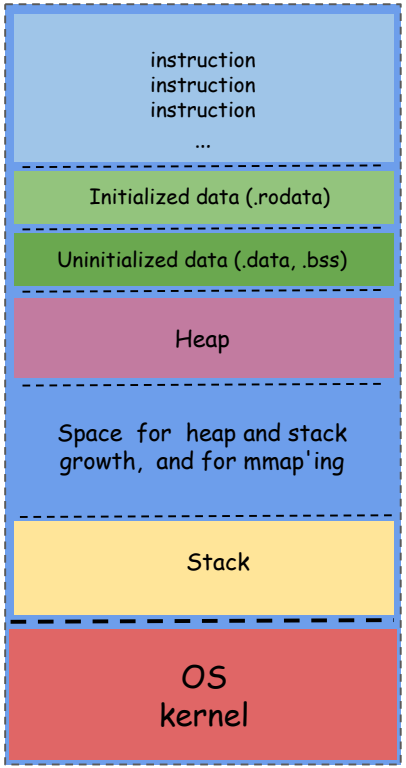

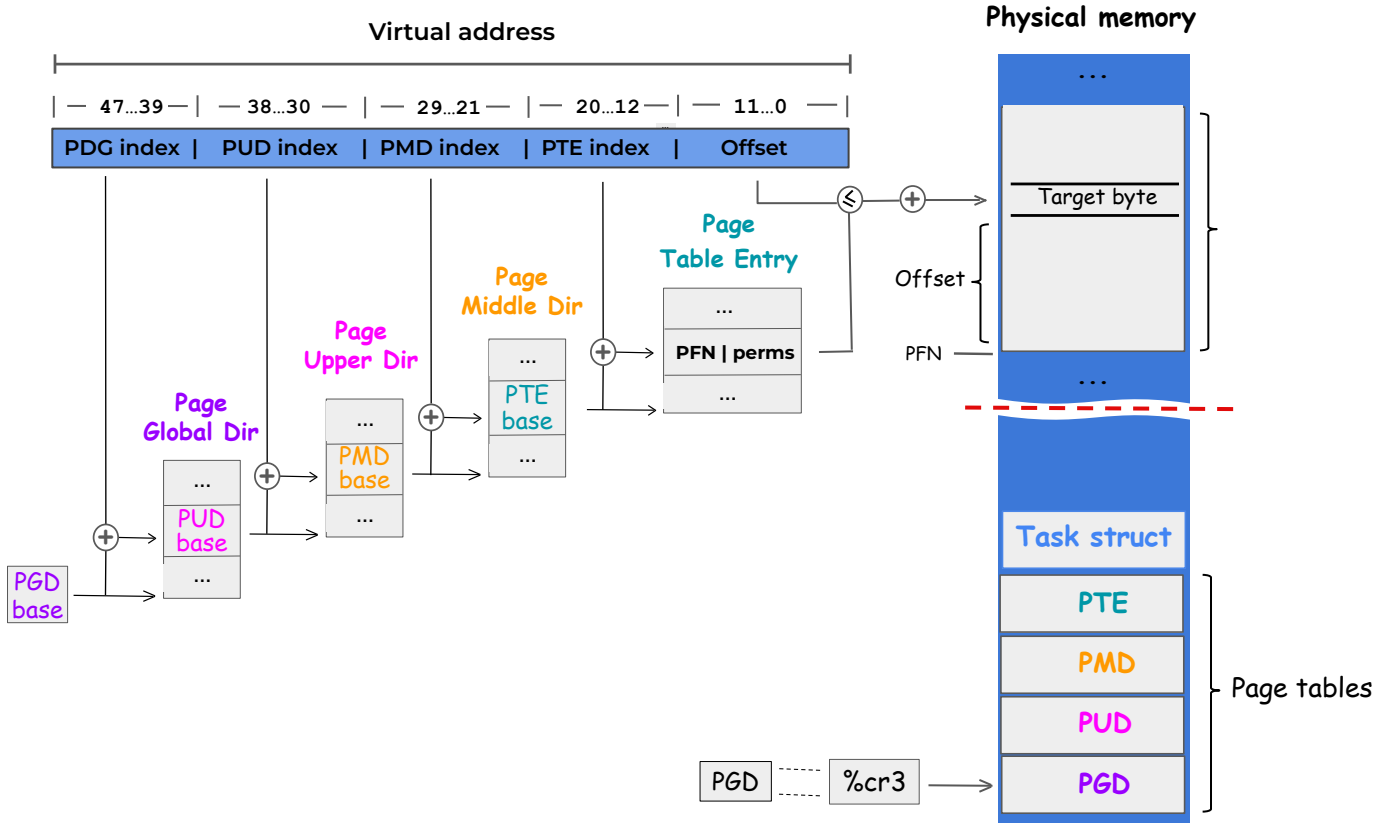

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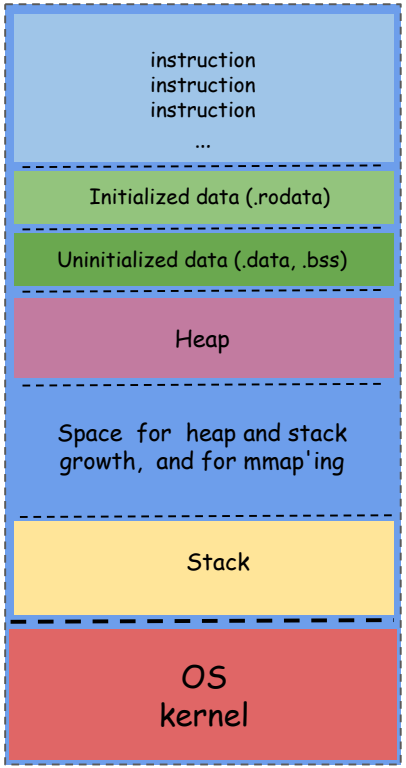


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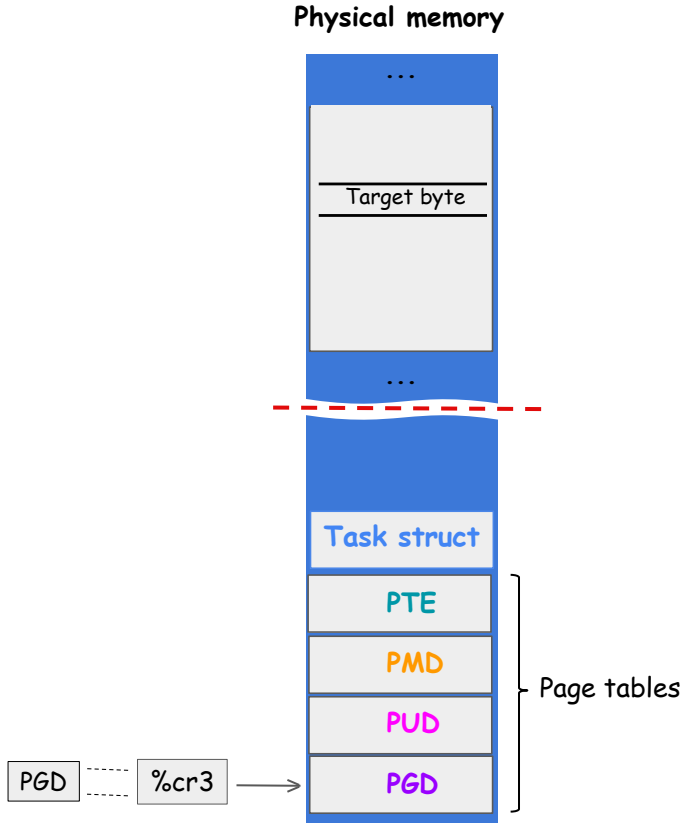
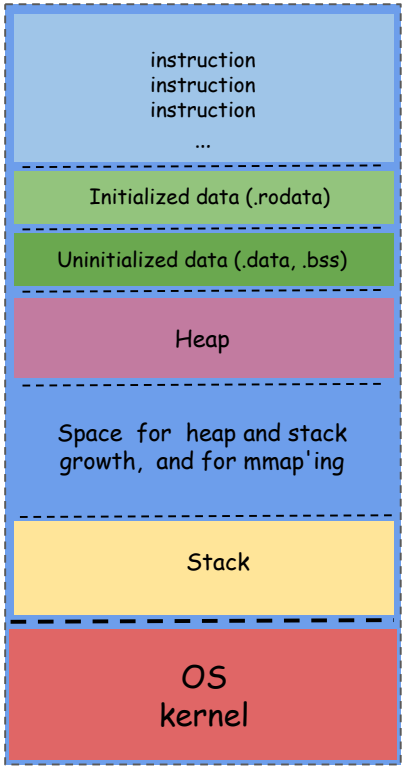


Putting it all together: (3/3) System-wide page frame allocators



> Buddy memory allocator
- Physical memory is divided into "zones"
- Buddy allocator: Range-based, power-of-2 allocator
- Each zone has its own buddy allocator instance to manage free physical pages

>> Request comes in
- Allocator finds the smallest block that fits
- Only larger blocks available? Splits them into "buddies" until the right size is reached